

NALAA

Hamburg 10G

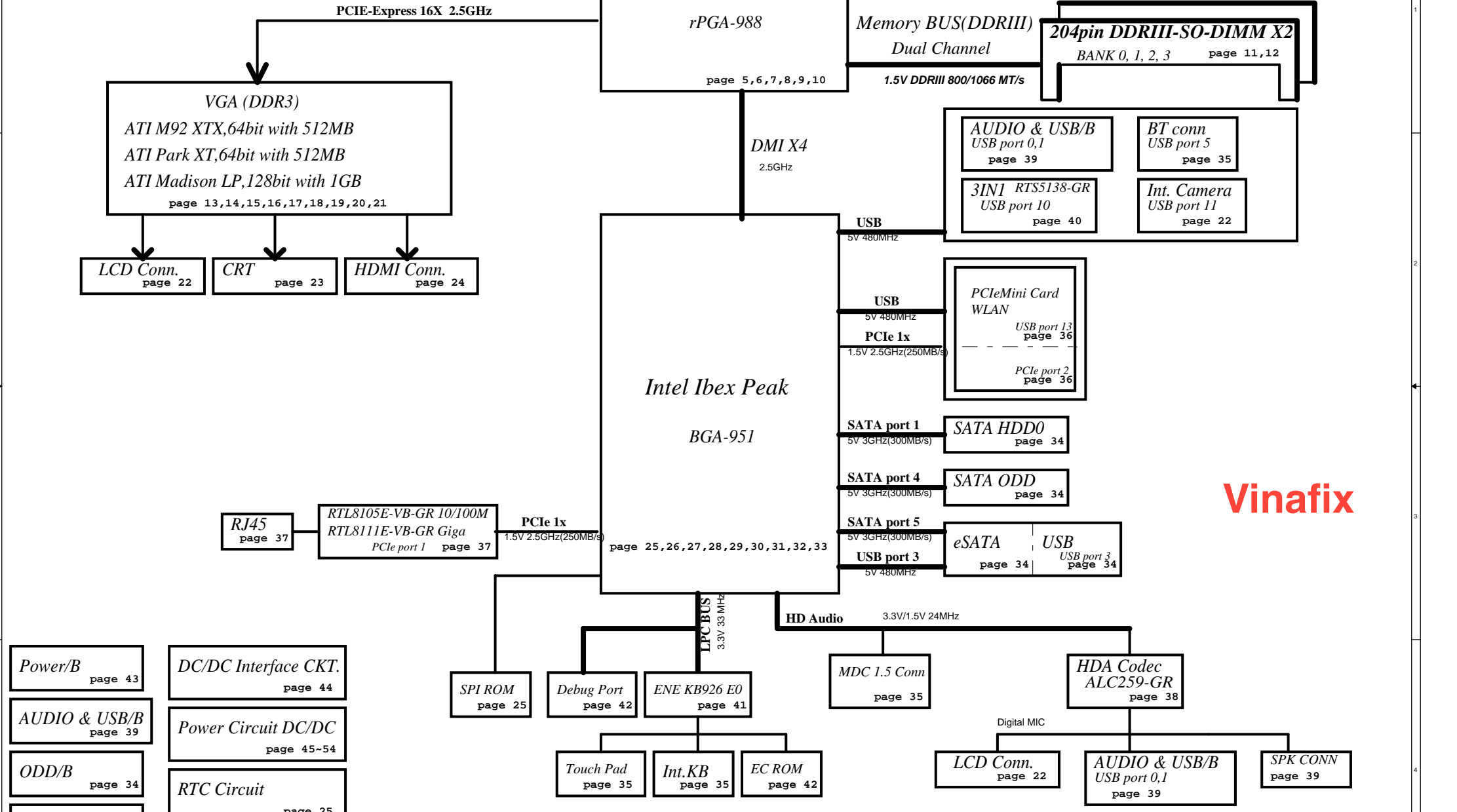
LA-6042P REV 1.0 Schematic

**Intel Arrandale / IBEX PEAK
2010-04-12 Rev 1.0**

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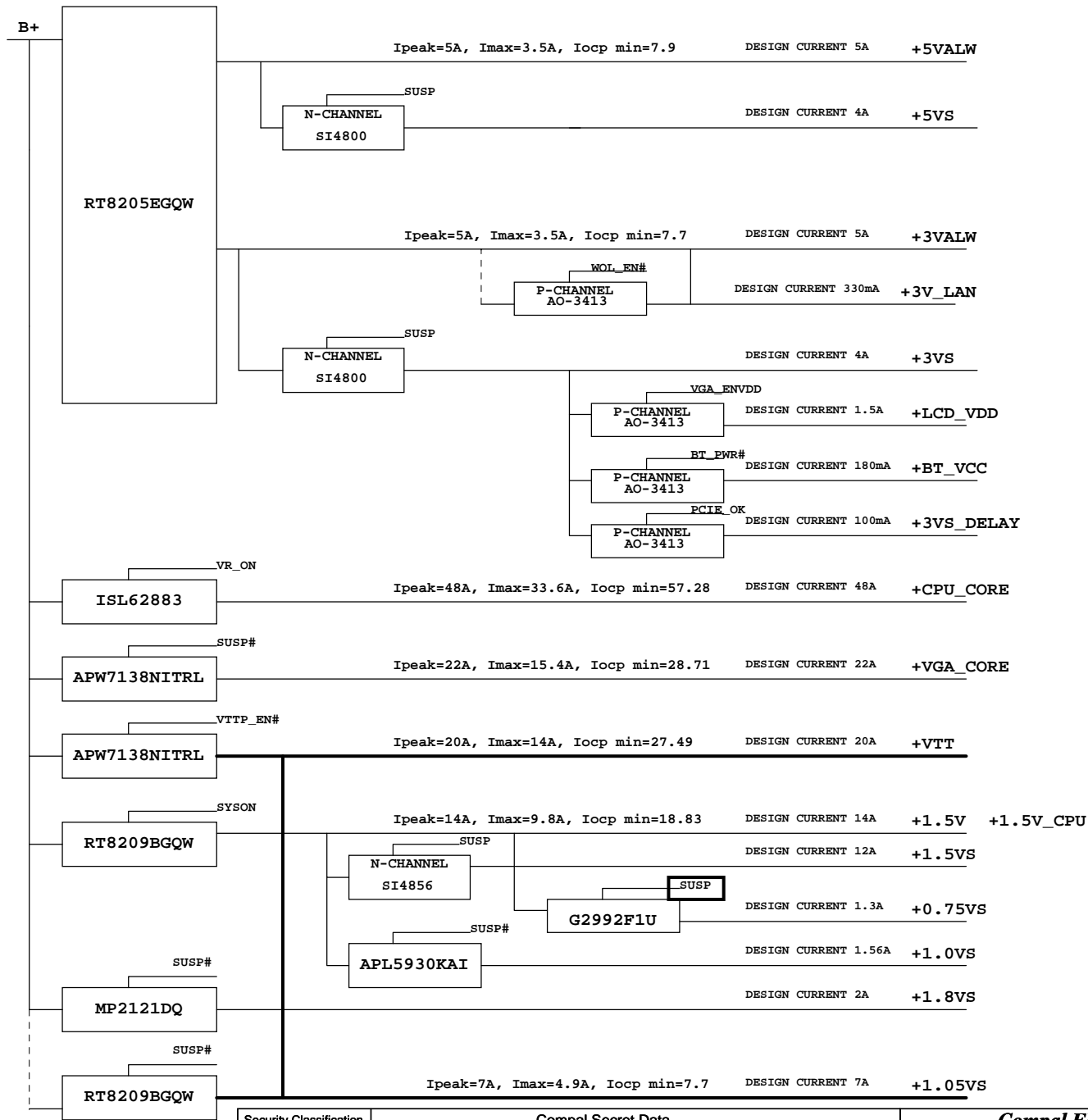
Compal Confidential

Model Name : NALAA
File Name : LA-6042P



Vinafix

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW +1.5VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.0VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

CPU	Arrandale				Clarksfield			
S3 Reduce	Enable		Disable		Enable		Disable	
GPU Type	Manhattan	M9X	Manhattan	M9X	Manhattan	M9X	Manhattan	M9X
BTO	M1@ PS@ MANHA@	M1@ PS@ M9X@	M1@ NPS@ MANHA@	M1@ NPS@ M9X@	PSM3@ PS@ MANHA@	PSM3@ PS@ M9X@	M3@ NPS@ MANHA@	M3@ NPS@ M9X@

Function	PCH			GPU			
description	(H5)	(H7)		(P5)	(PX5)	(M1)	(925)
explain	HM55	HM57	PM55	Park LP	Park XT	Madison LP	M92 XTX
BTO	HM55R3@	HM57R3@		PARKLP@	PARKXT@	MADISONLP@	M92XTXR3@

Function	LAN		HDMI		Bluetooth	MODEM
description	(E)	(C)	(Y)	(Q)	(B)	(R)
explain	10/100M	Giga	HDMI	Non-HDMI	Bluetooth	MDC
BTO	8105E@	8111E@	HDMI@		BT@	MDC@

Function	VRAM		DC JACK
description			
explain	512M	1G	DC JACK
BTO	4PCS@	8PCS@	45@

EC SM Bus1 address

EC SM Bus2 address

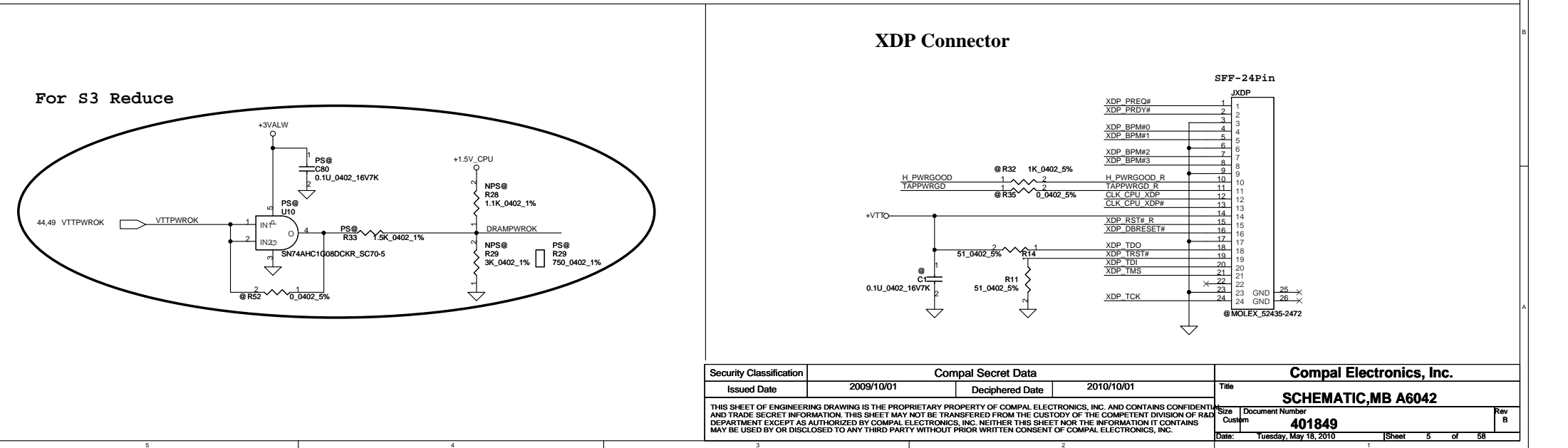
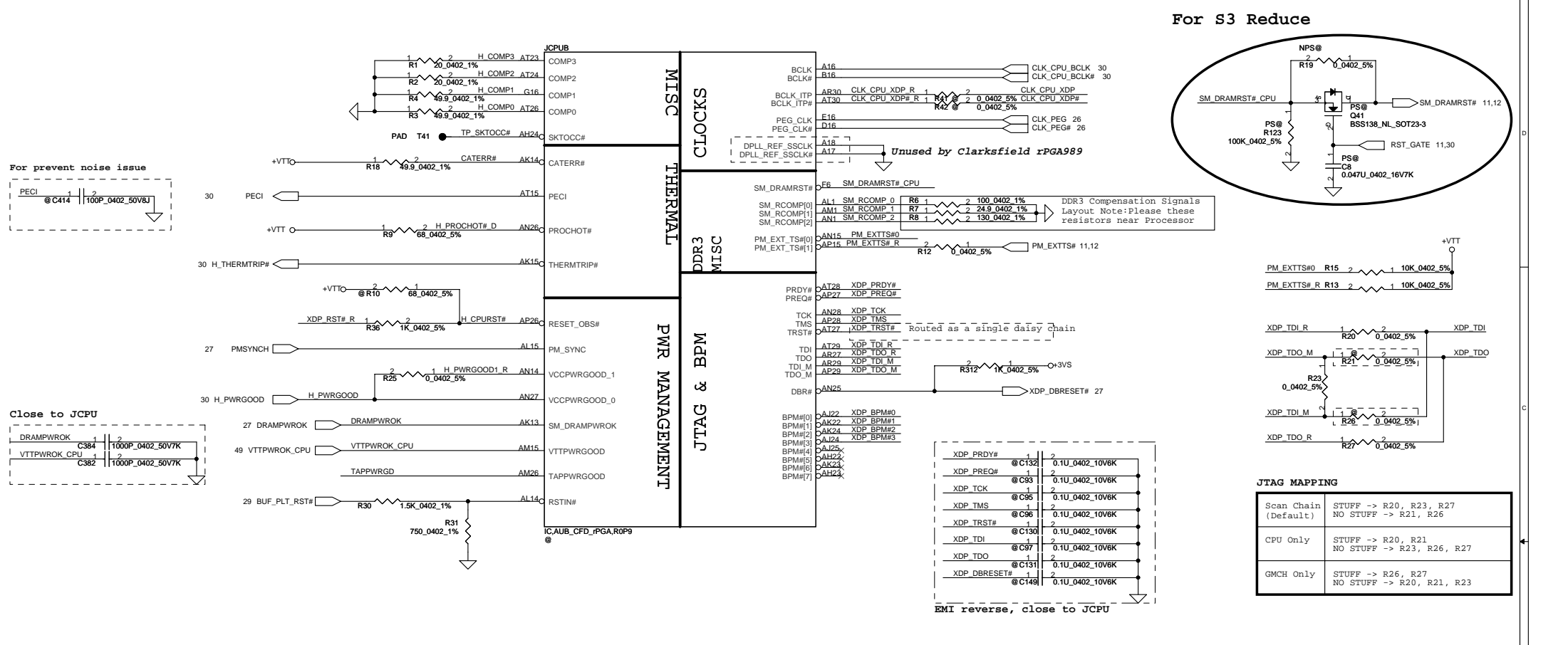
Power	Device	Address	Power	Device	Address
+3VALW	EC KB926 D3		+3VS	EC KB926 D3	
+3VALW	Smart Battery	0001 011x b	+3VS	VGA THM Sensor ADM1032ARMZ	1001 110x b
			+3VS	PCH	0100 110x b

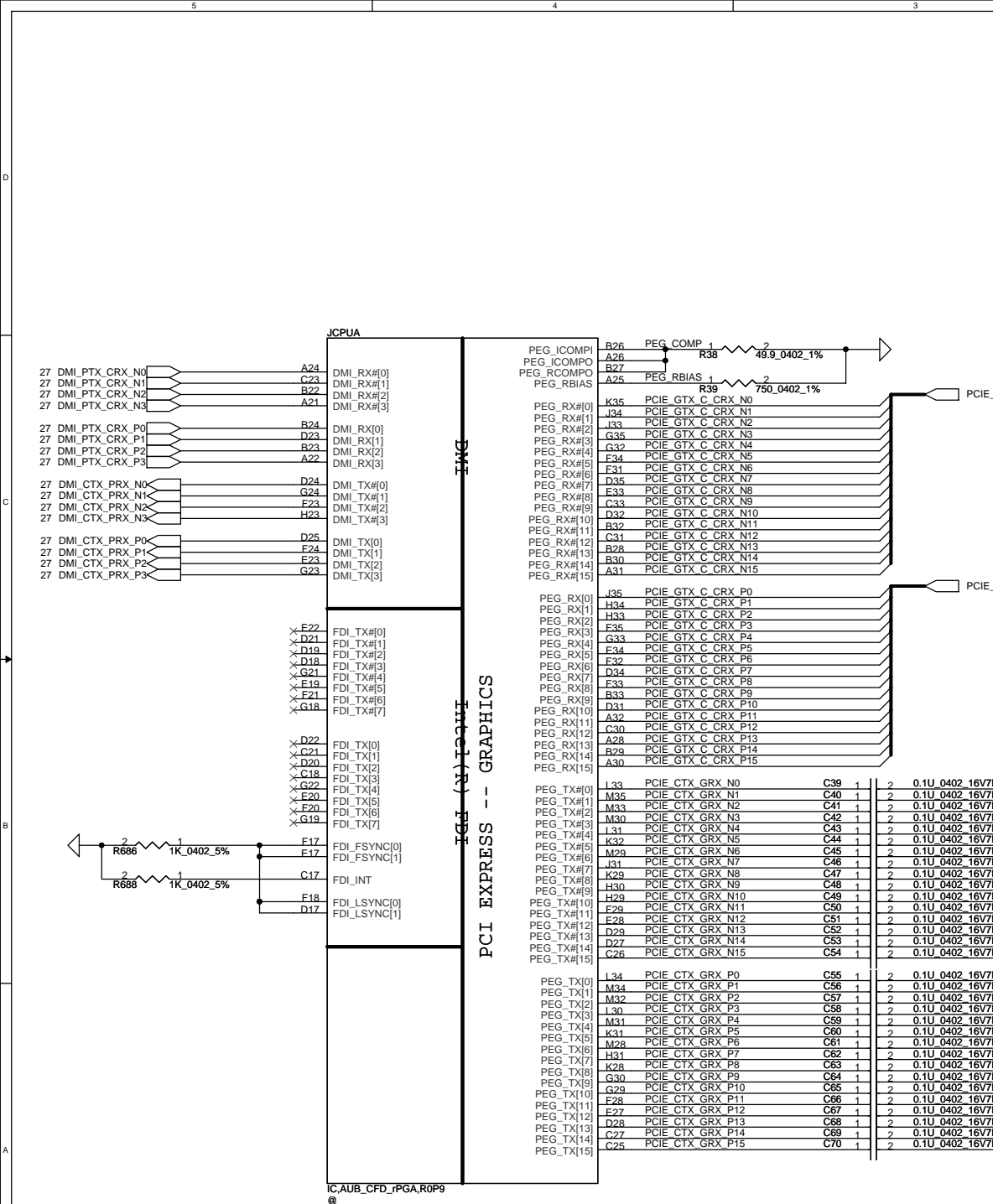
PCH SM Bus address

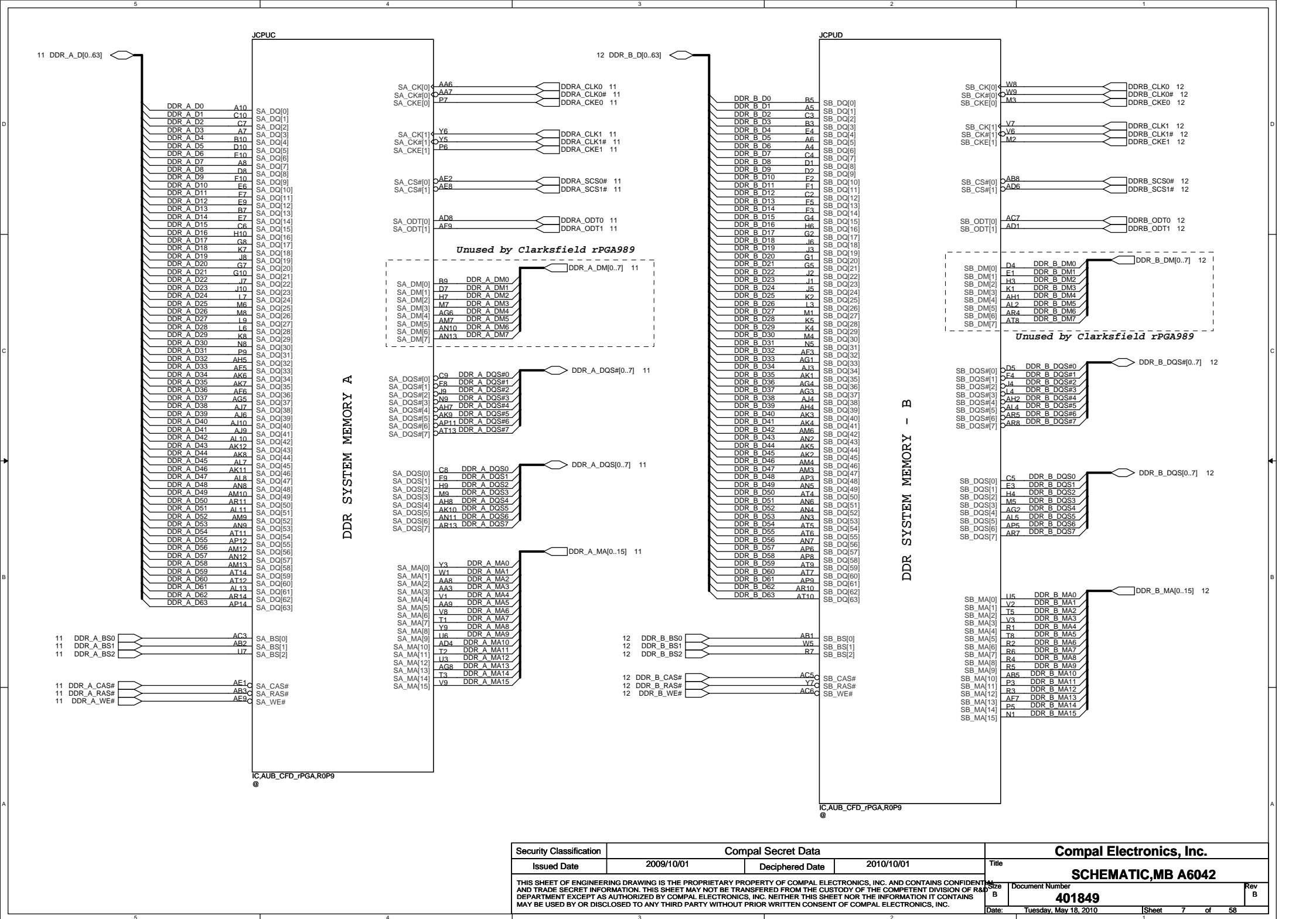
Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	WLAN	

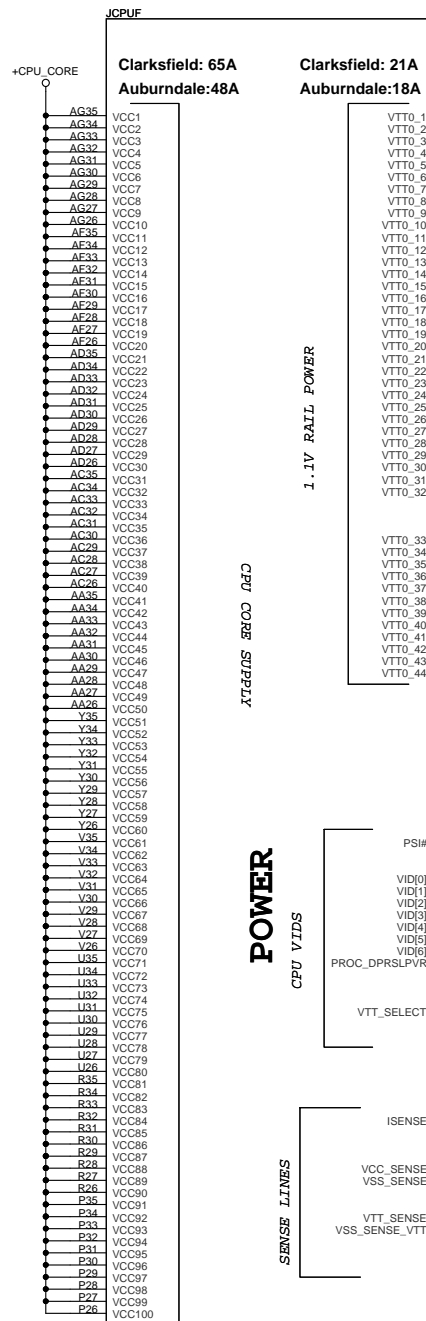
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH	HIGH
S3(Suspend to RAM)		LOW	HIGH	HIGH
S4(Suspend to Disk)		LOW	LOW	HIGH
S5(Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

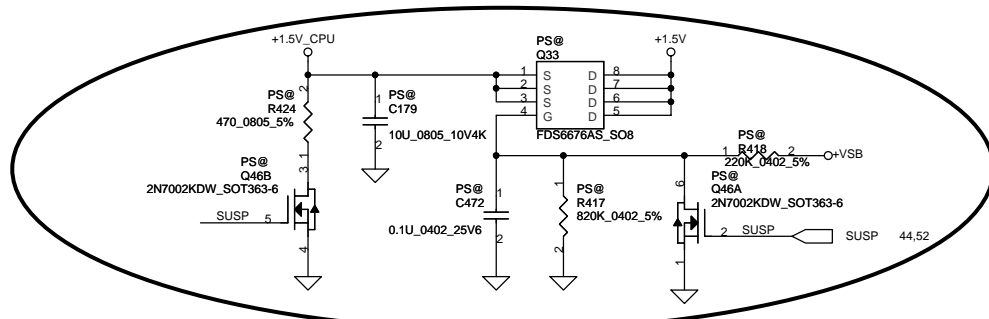
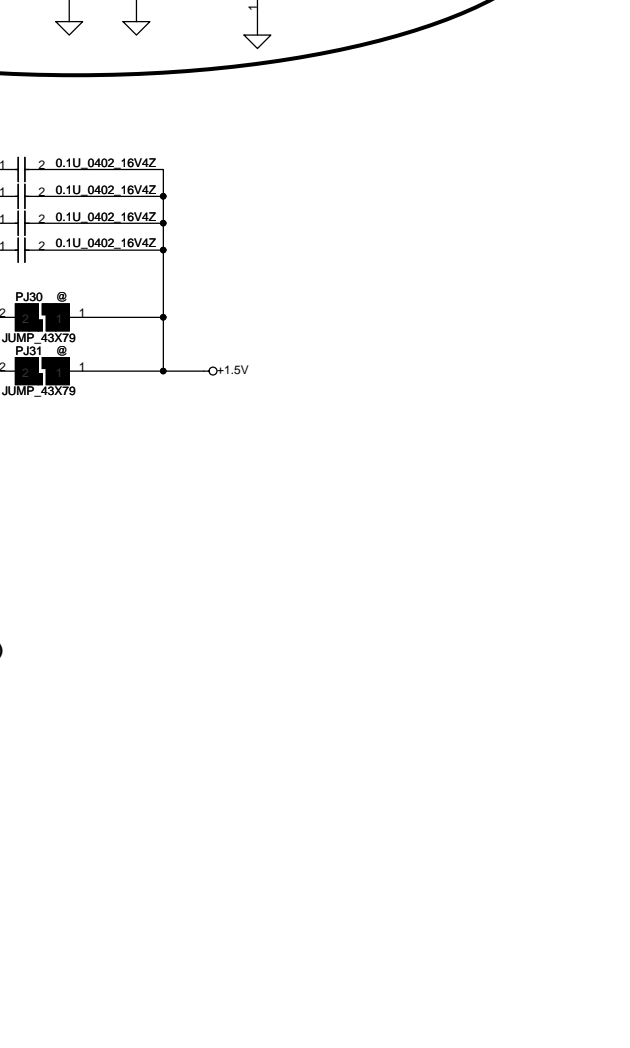
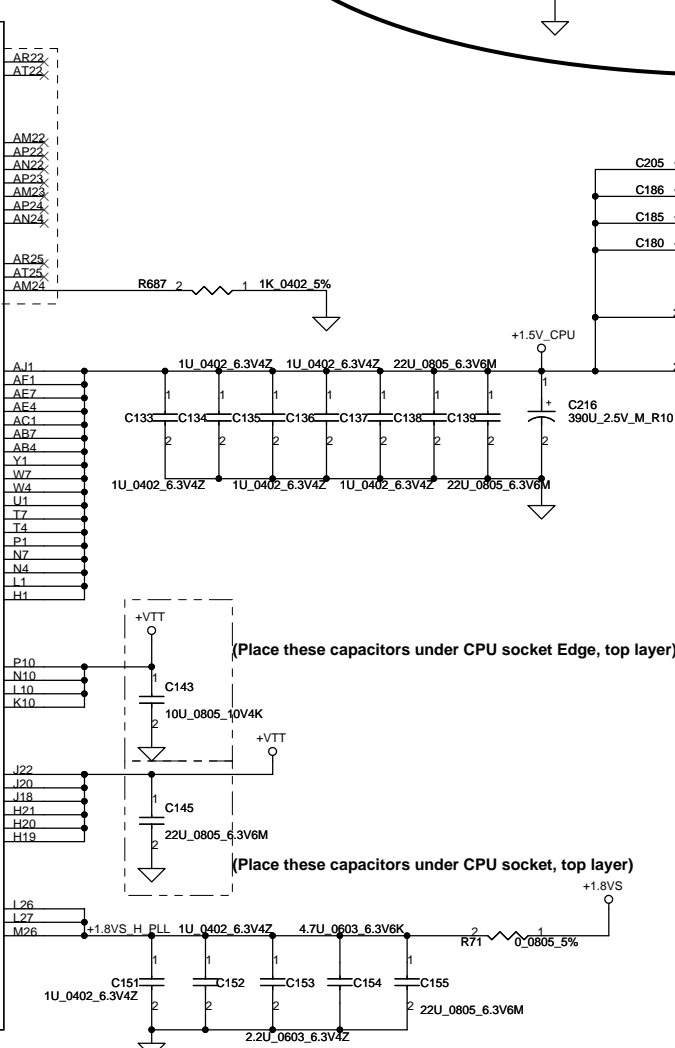
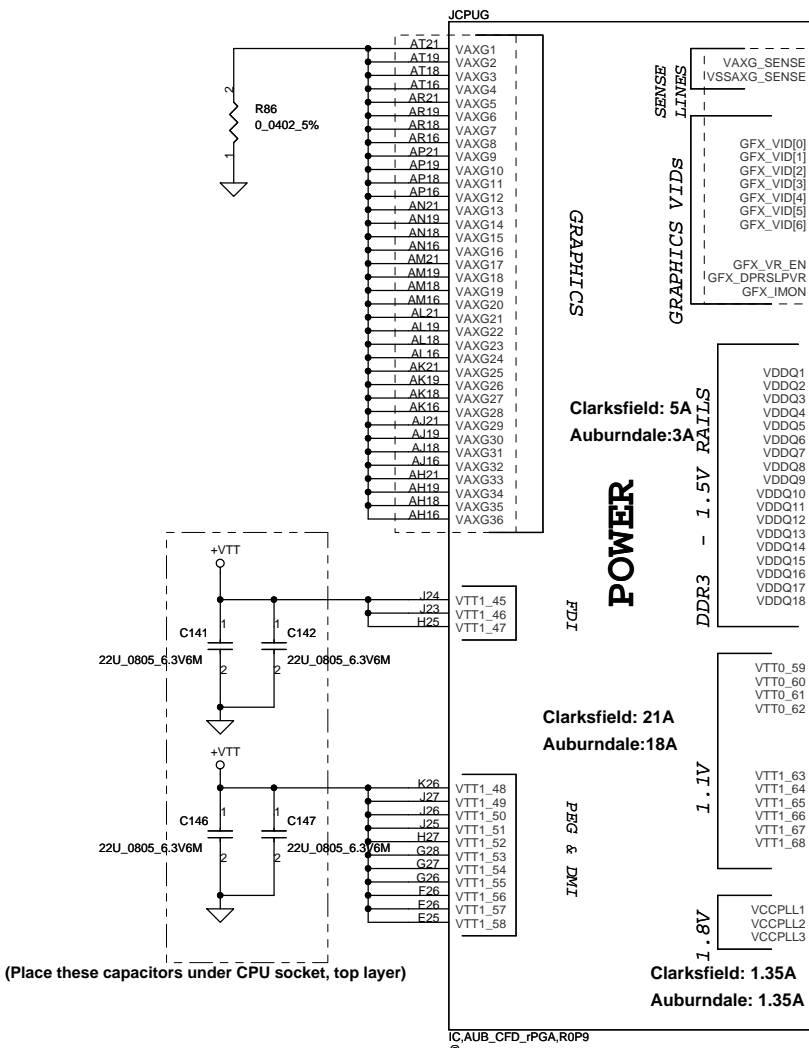
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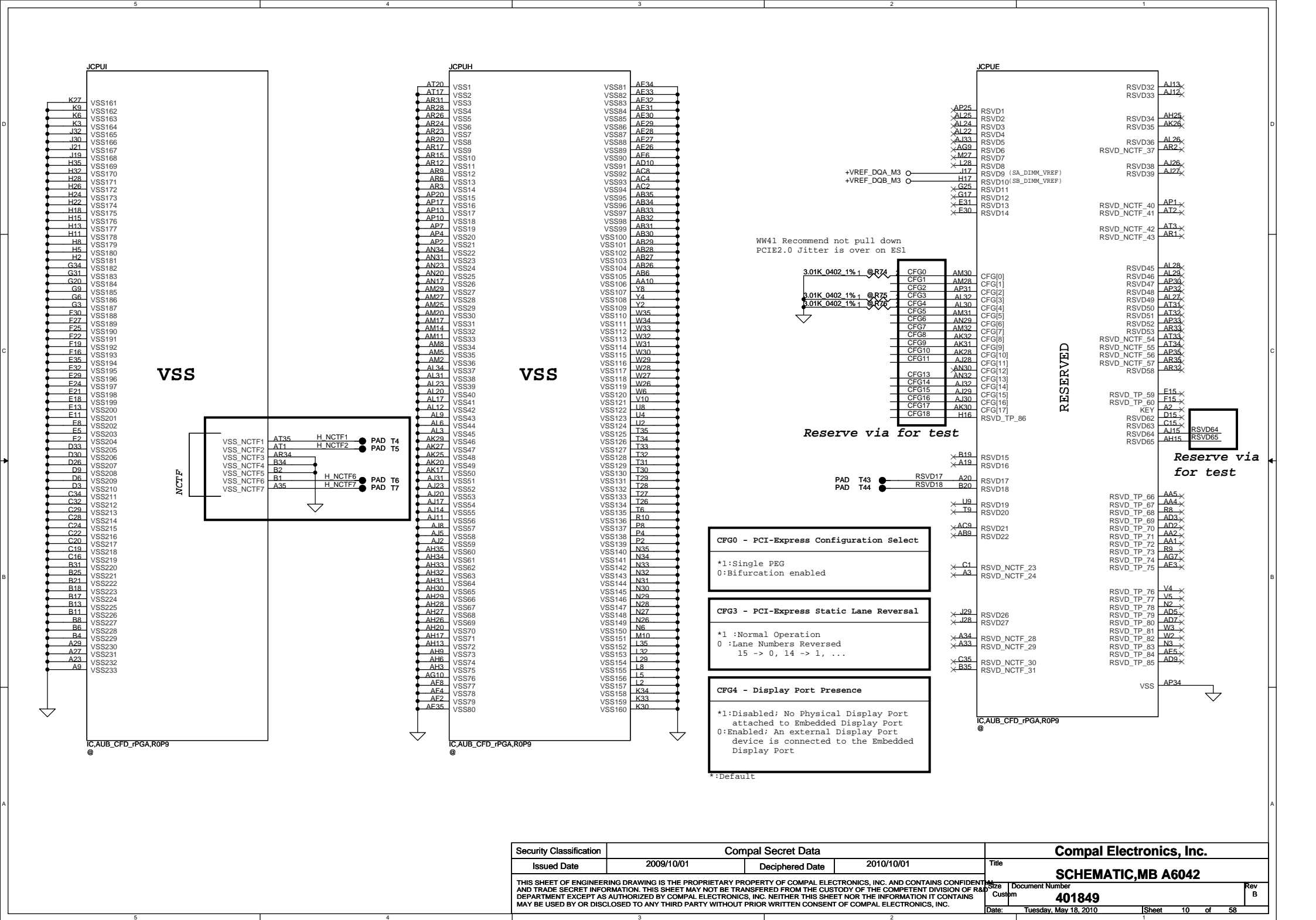


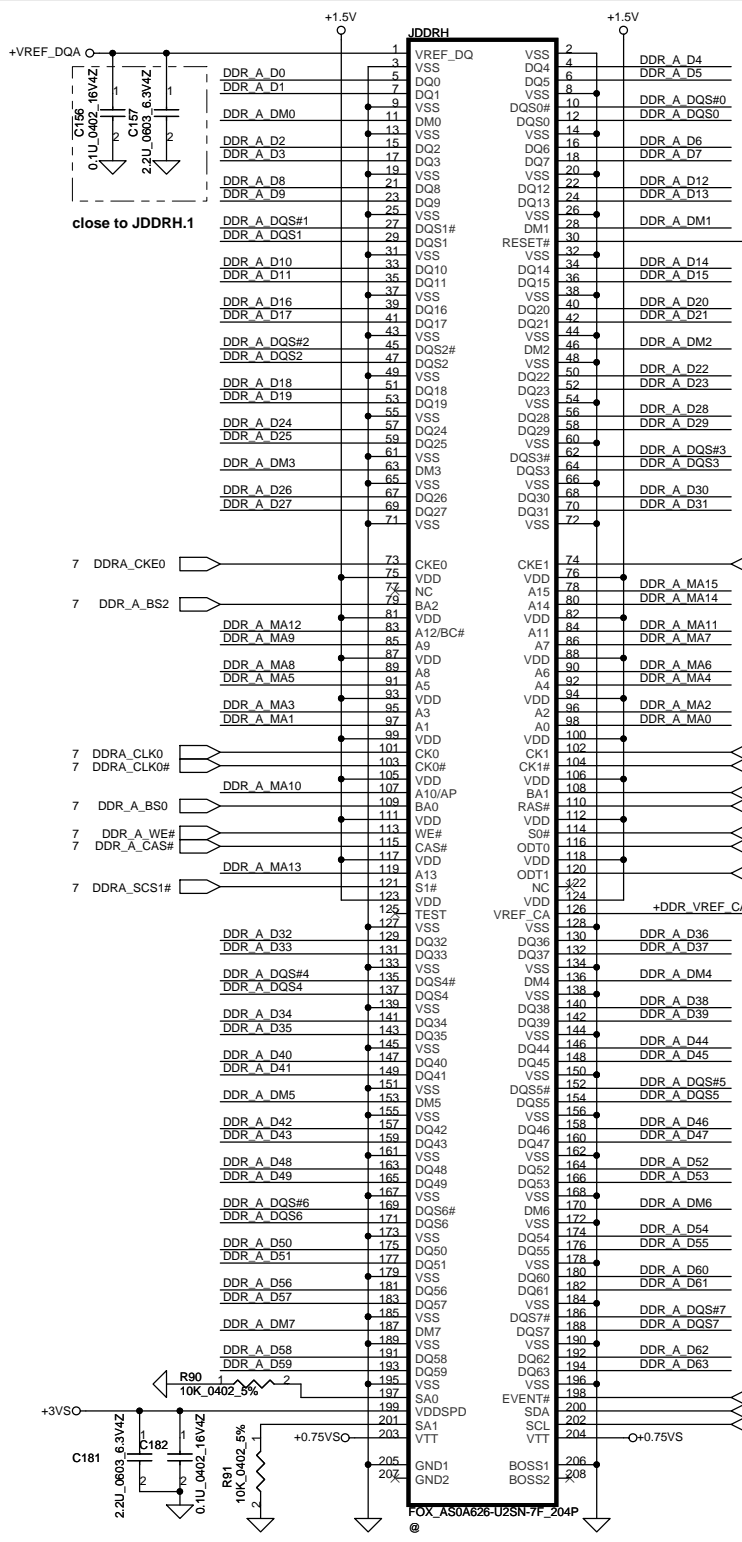
(Place these capacitors under CPU socket, top layer)

(Place these capacitors under CPU socket Edge, top layer)

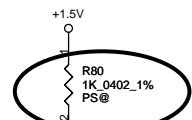
(Place these capacitors under CPU socket, top layer)

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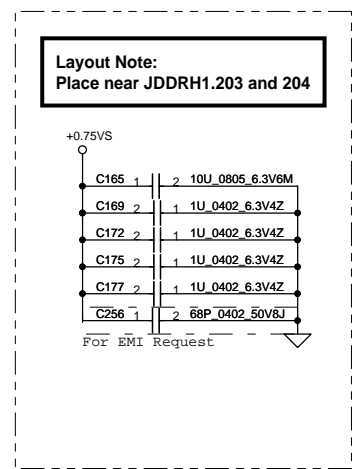
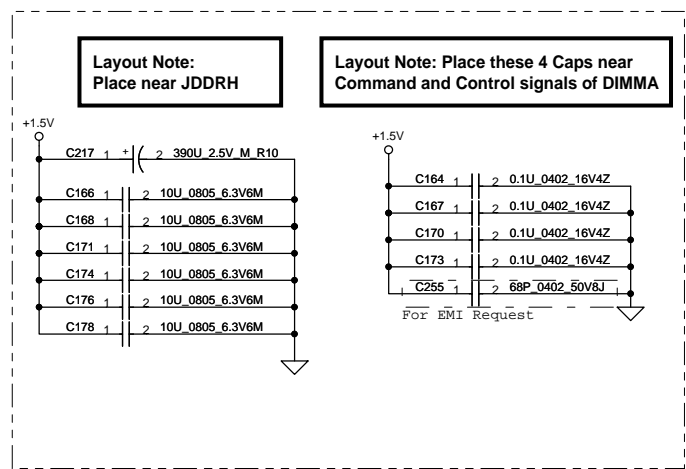
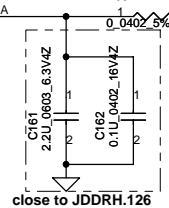
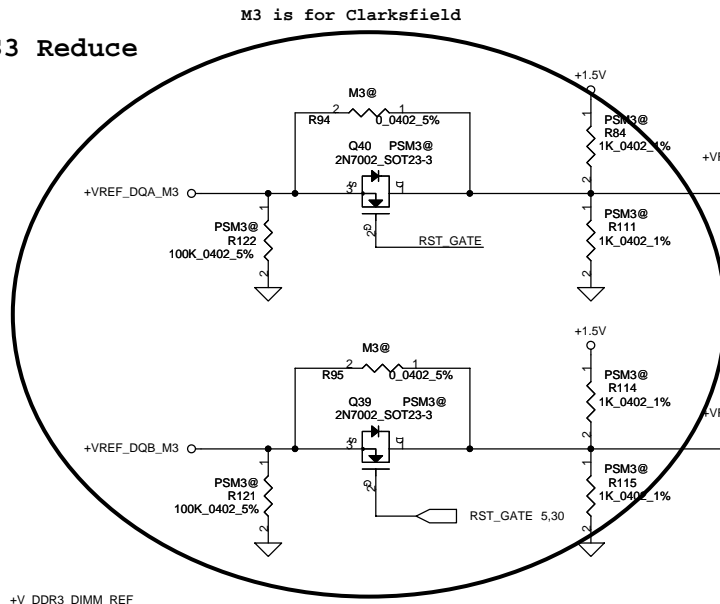


DDR3 SO-DIMM A Reverse Type



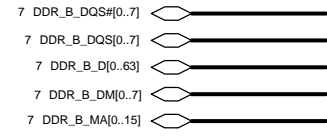
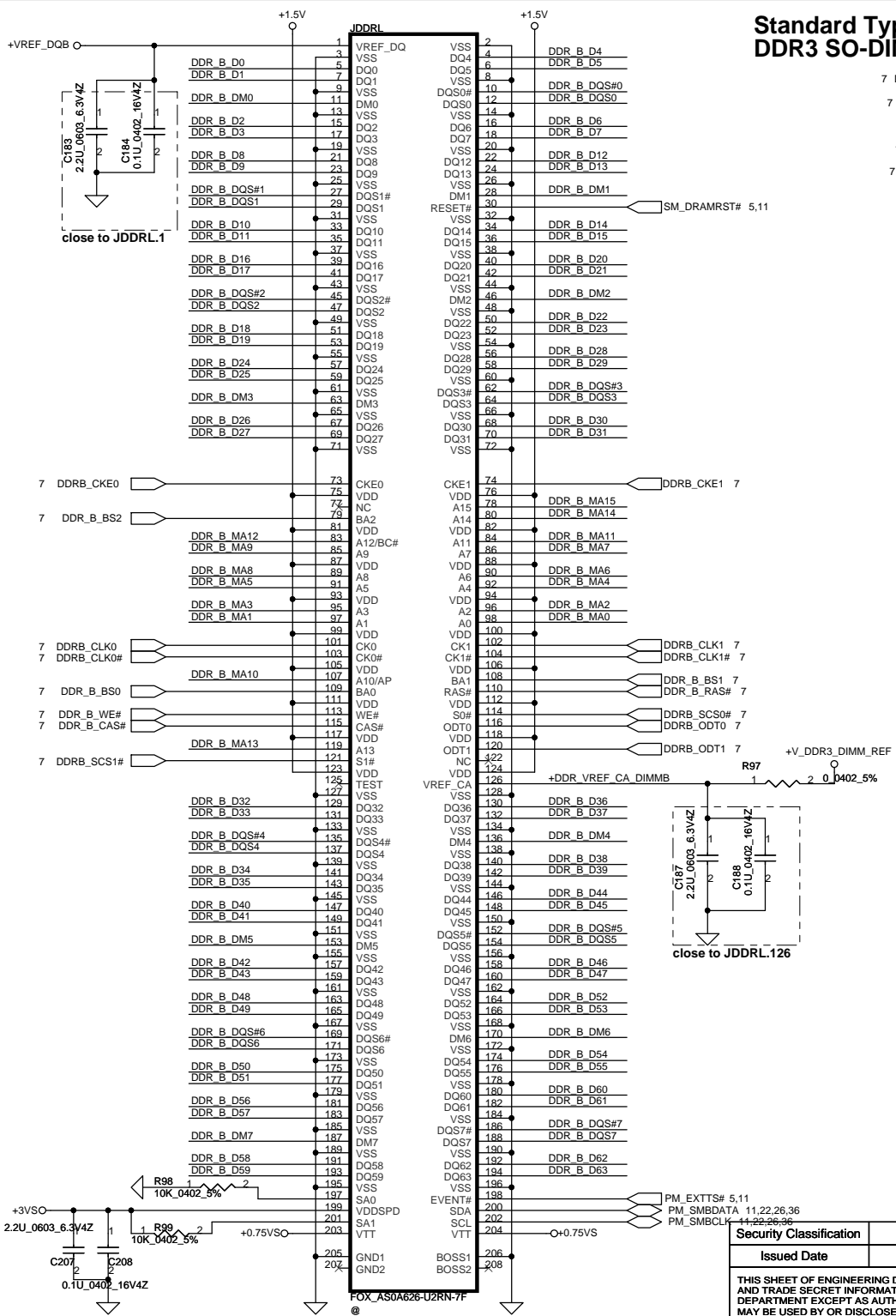
- 7 DDR_A_DQS[0..7]
- 7 DDR_A_DQS#0[0..7]
- 7 DDR_A_D[0..63]
- 7 DDR_A_DM[0..7]
- 7 DDR_A_MA[0..15]

For S3 Reduce

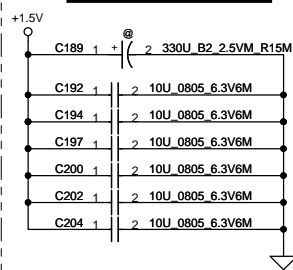


12-22-26-36													
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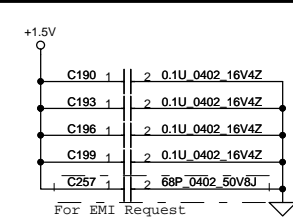
Standard Type DDR3 SO-DIMM B



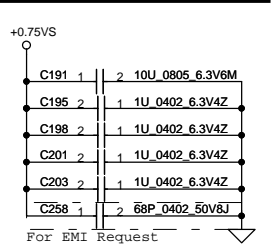
Layout Note:
Place near JDDRRL



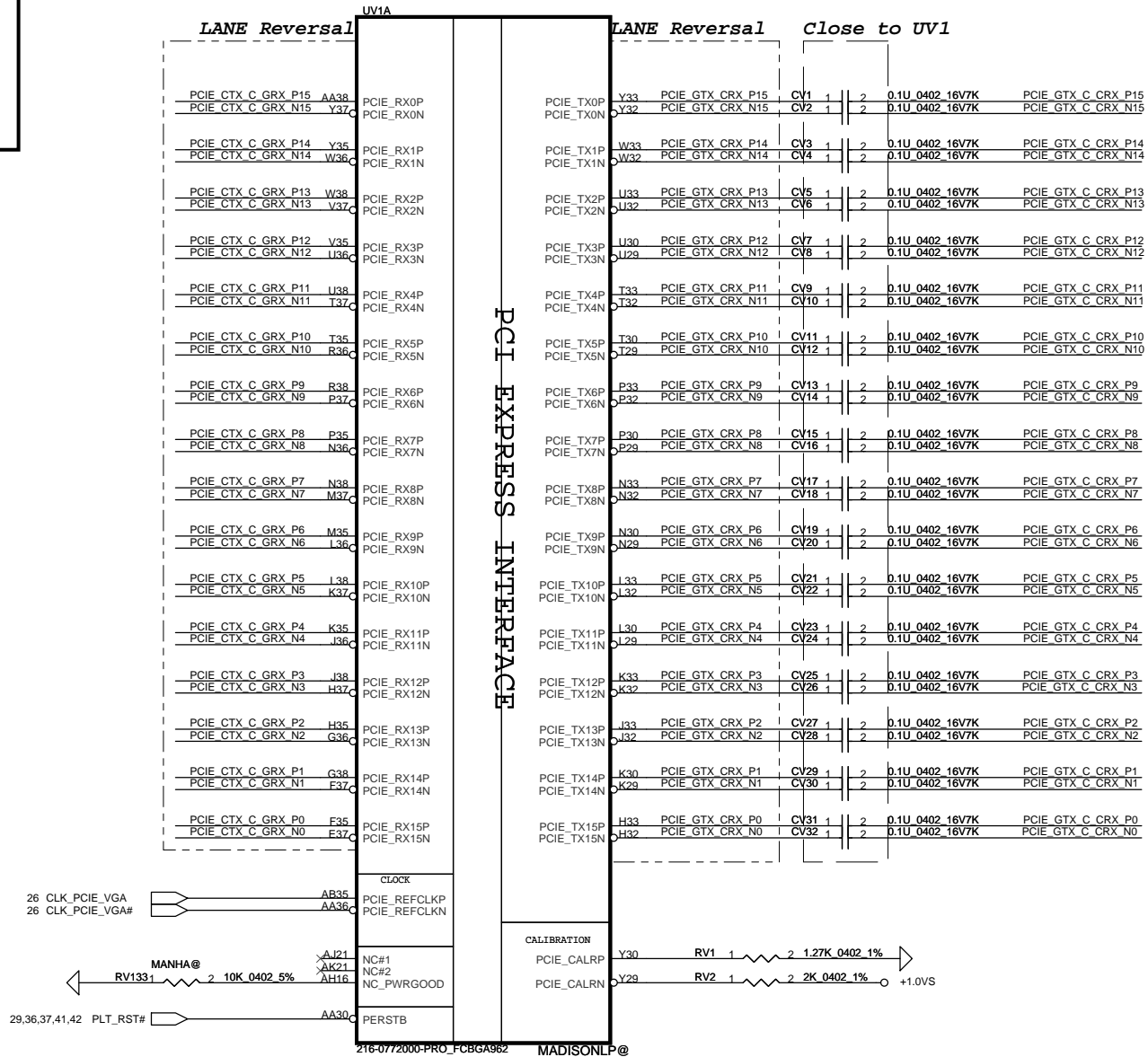
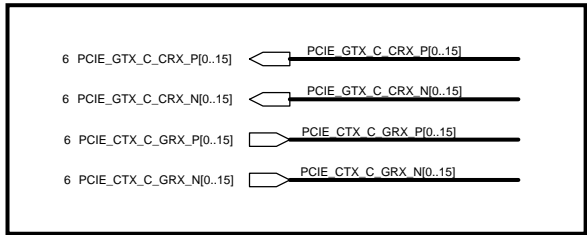
Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB



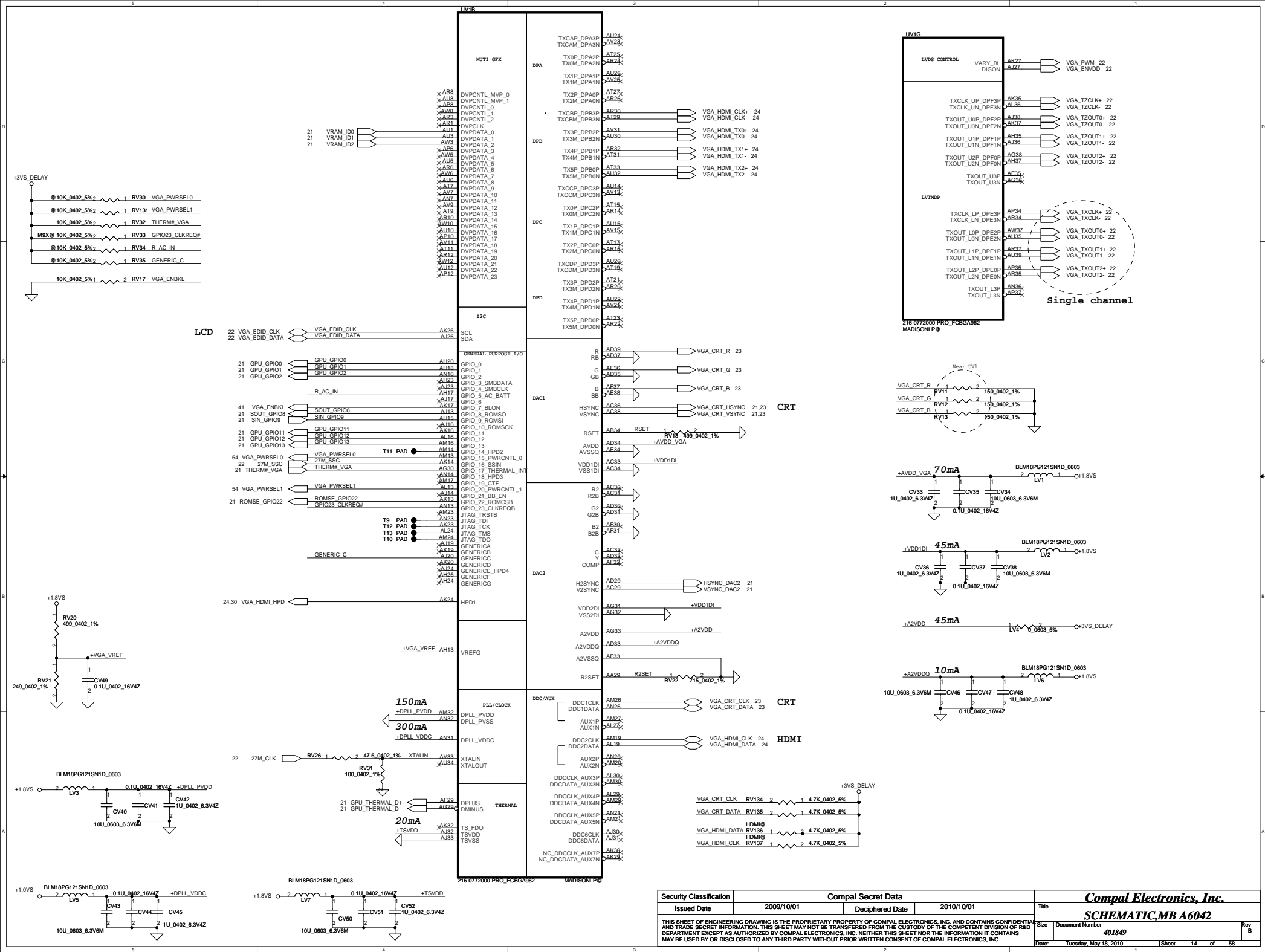
Layout Note:
Place near JDDRRL.203 and 204

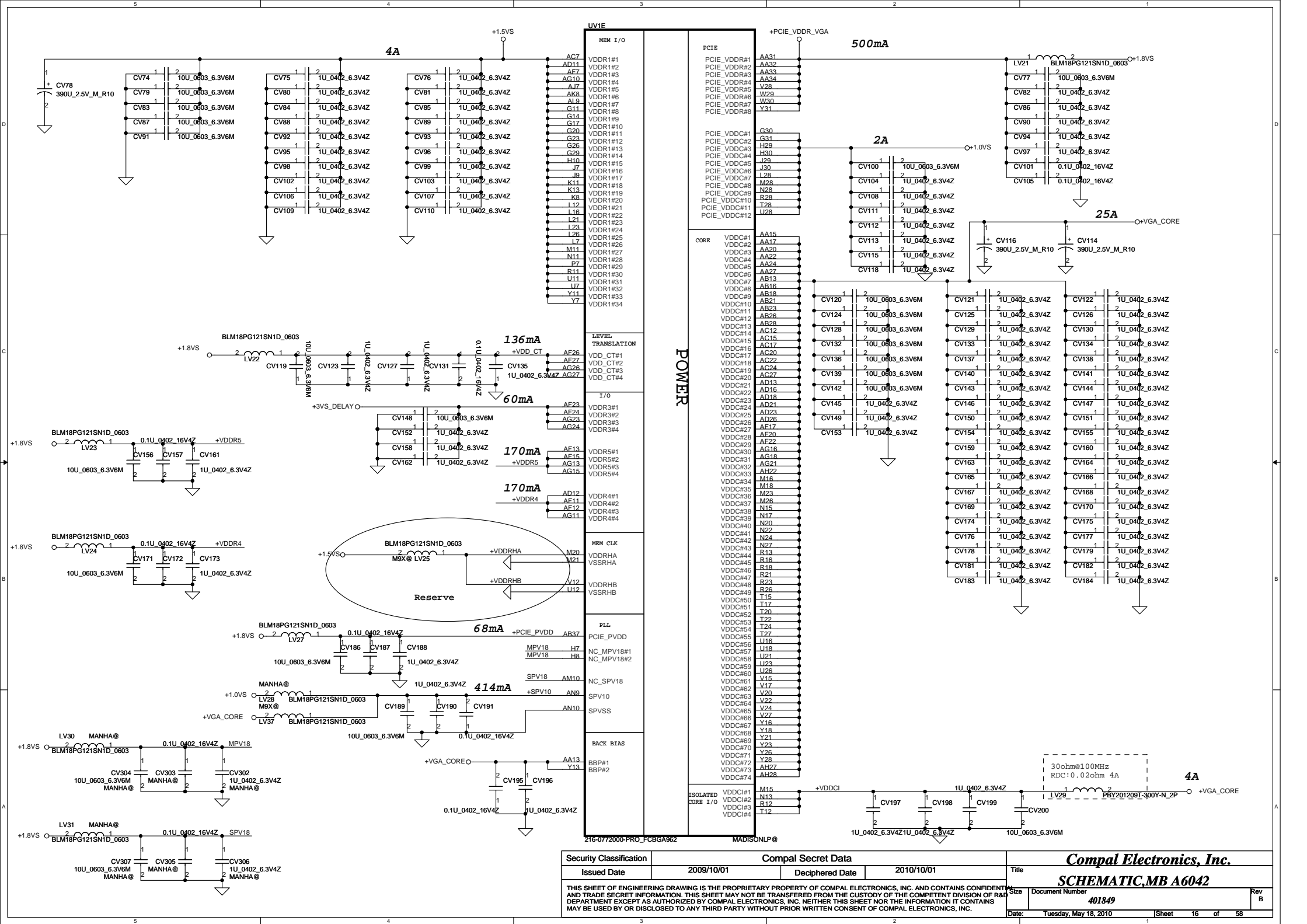


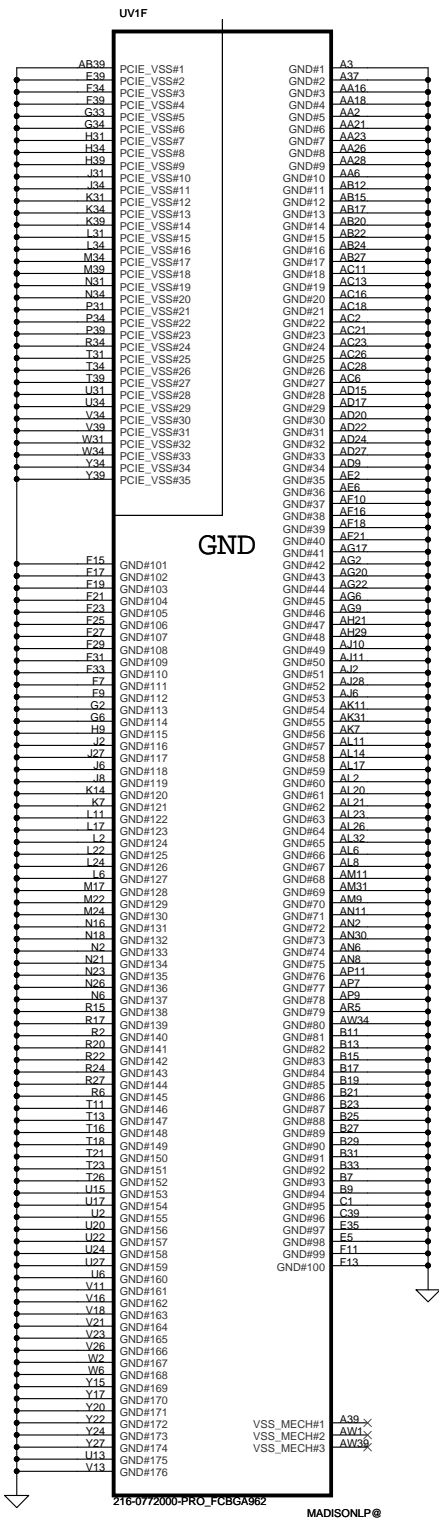
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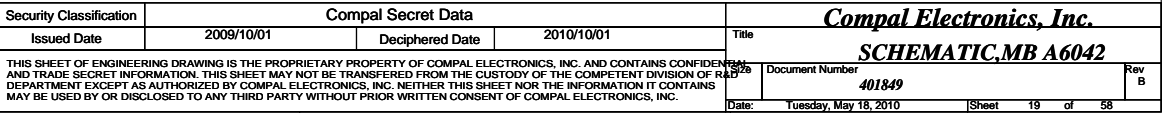
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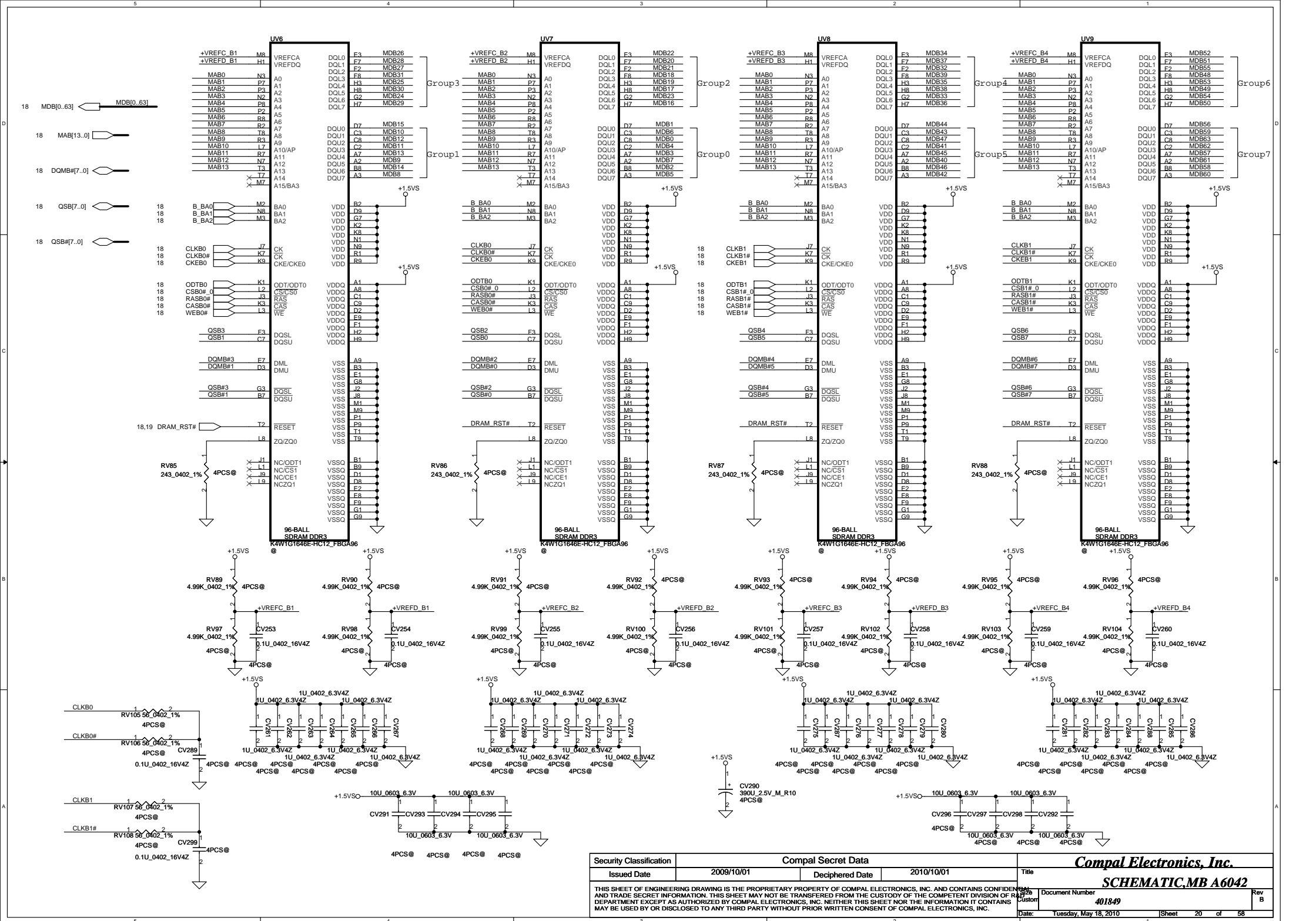




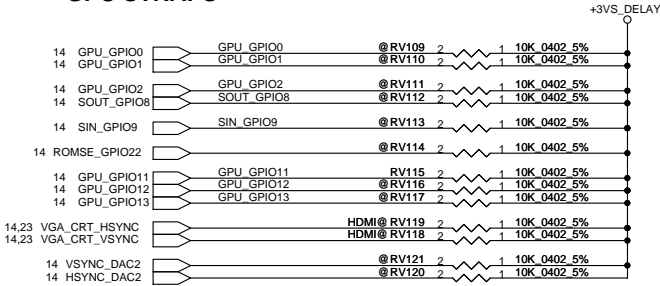


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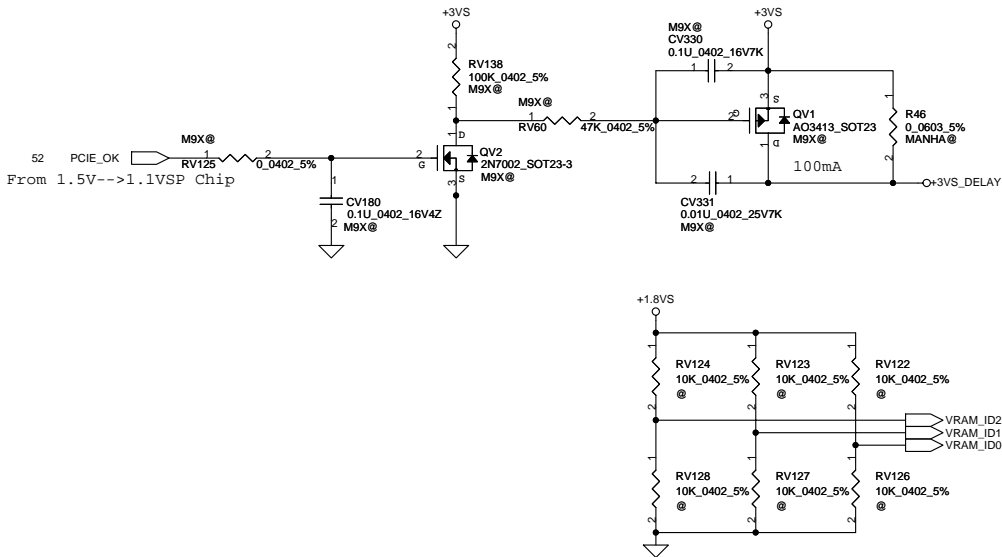
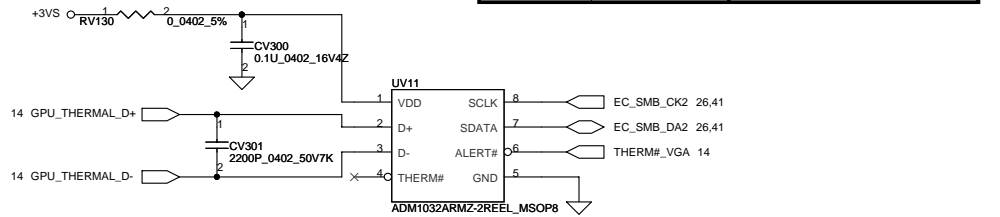


GPU STRAPS



GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0 (M25P05A)
0 0 1	256MB	
0 1 0	64MB	

External VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

Straps Name	Pin Name	Net Name	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPU_GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	GPU_GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	GPU_GPIO2	PCIe GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
RESERVED	GPIO_8_ROMSO	SOUT_GPIO8	RESERVED	0
BIF_VGA DIS	GPIO_9_ROMSI	SIN_GPIO9	VGA Controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Enable)
RESERVED	GPIO_21_BB_EN	N.C	RESERVED	0 (Internal pulldown)
BIOS_ROM_EN	GPIO_22_ROMCSB	ROMSE_GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
ROMIDCFG(2:0)	GPIOQ[13:11]	GPU_GPIO11 GPU_GPIO12 GPU_GPIO13	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	VSYN_C_DAC2	VIP Device Strap Enable indicates to the software driver 0 - Driver would ignore the value sampled on VHAD_0 during reset 1 - Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device is connected	0
RESERVED	H2SYNC	HSYN_C_DAC2	RESERVED	0
AUD[1] AUD[0]	HSYN_C_VSYNC	VGA_CRT_HSYN_C VGA_CRT_VSYN_C	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	1 1
RESERVED	GENERIC_C	GENERIC_C	RESERVED	0

AMD RESERVED CONFIGURATION STRAPS

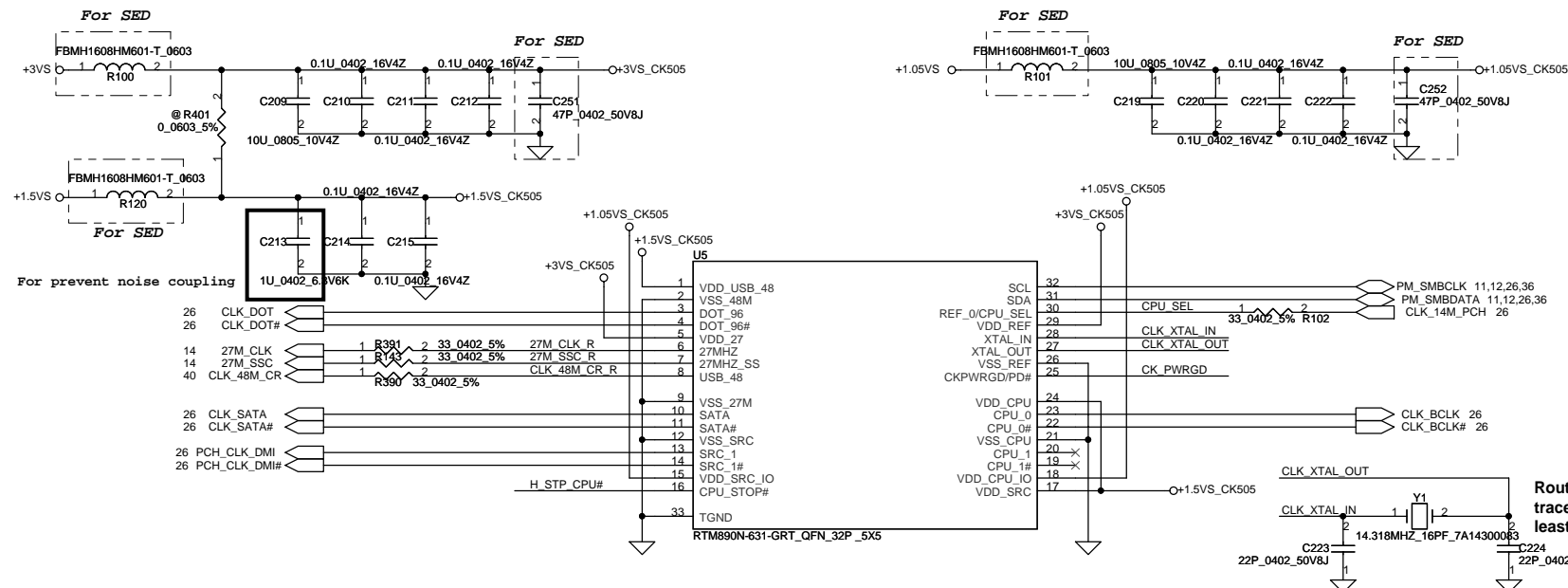
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
GPIO_8_ROMSO	GPIO_21_BB_EN

STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVPDATA (2,1,0)	Park M2 M92 GTX	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 0
			512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	0 0 1
			1G 128Mx16 (x4)	HYN		0 1 0 (Reserve)
			1G 128Mx16 (x4)	SAM K4W2G1646B-HC12	SA00003M000	0 1 1 (Reserve)
		Madison M2 M96 LP	1G 64Mx16 (x8)	HYN H5TQ1G63BFR-12C	SA000032400	1 0 0
			1G 64Mx16 (x8)	SAM K4W1G1646E-HC12	SA000035700	1 0 1
			2G 128Mx16 (x8)	HYN		1 1 0 (Reserve)
			2G 128Mx16 (x8)	SAM K4W2G1646B-HC12	SA00003M000	1 1 1 (Reserve)

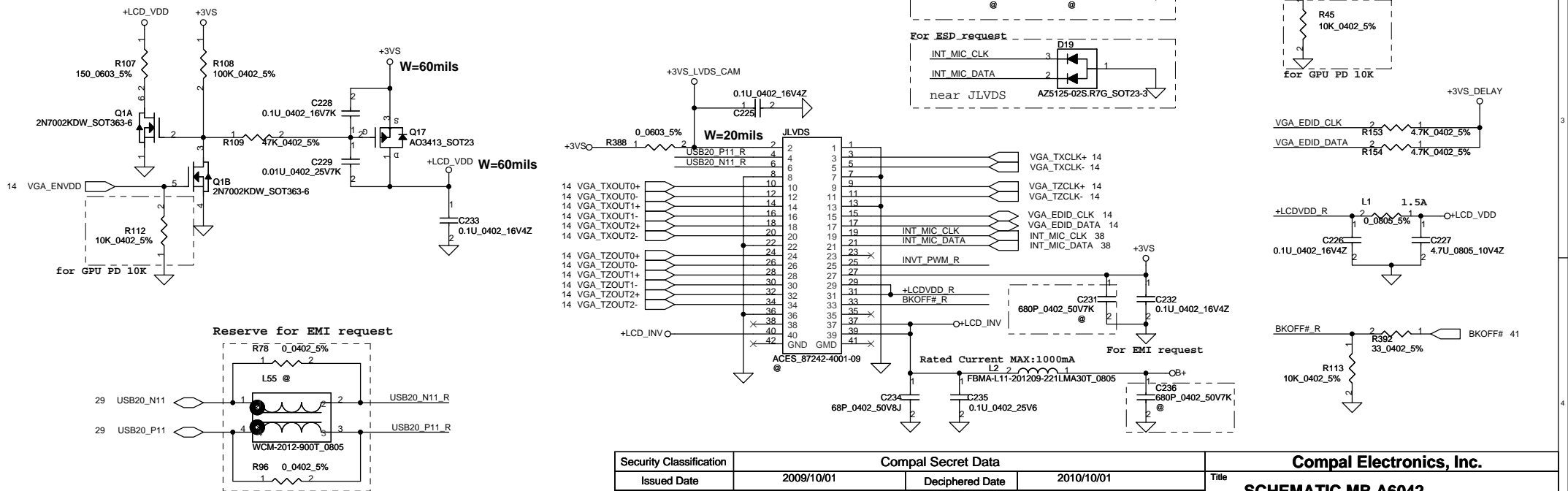
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Clock Generator

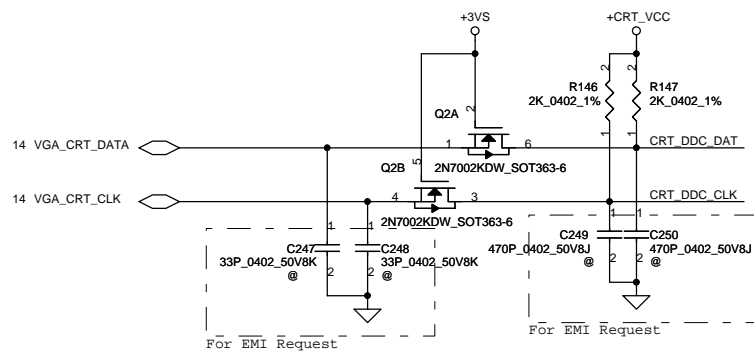
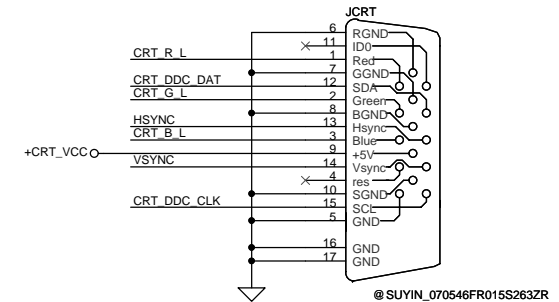
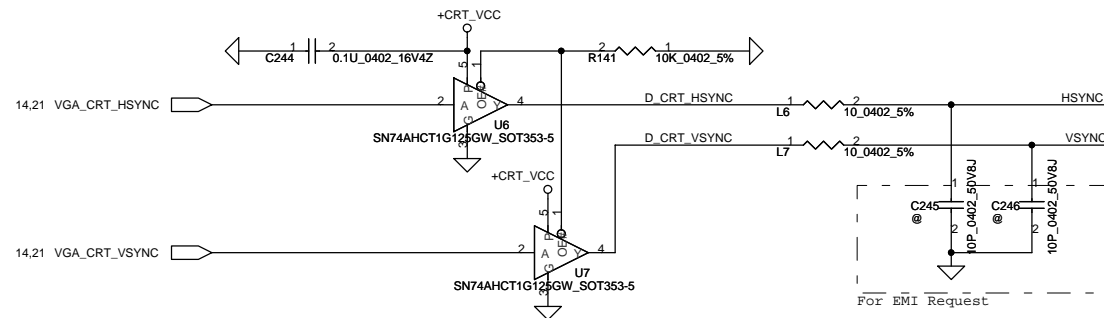
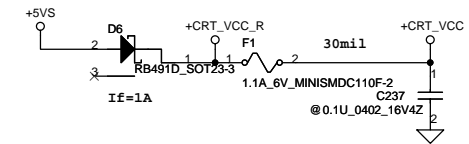
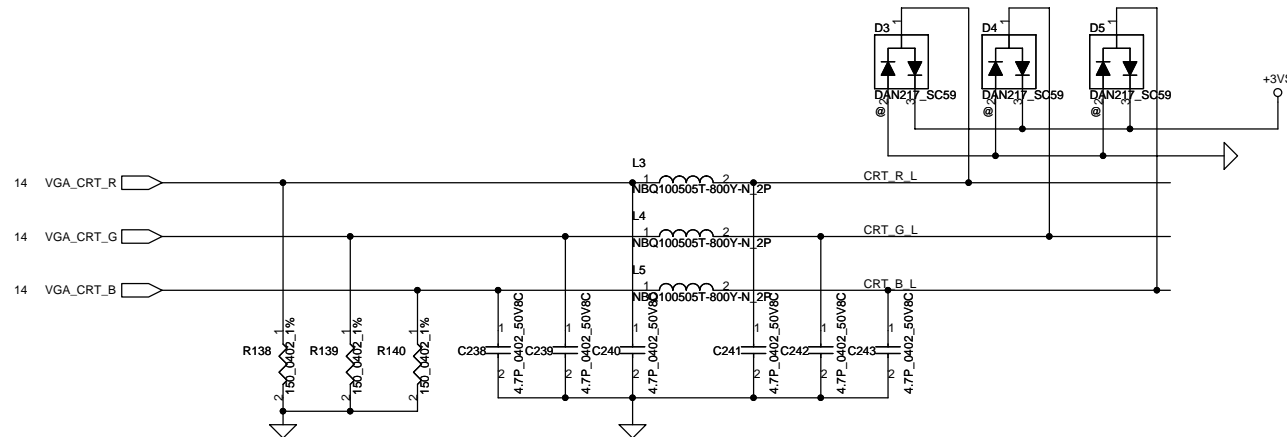


CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

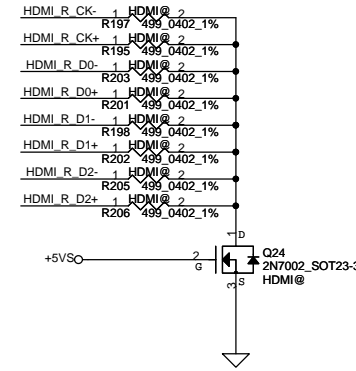
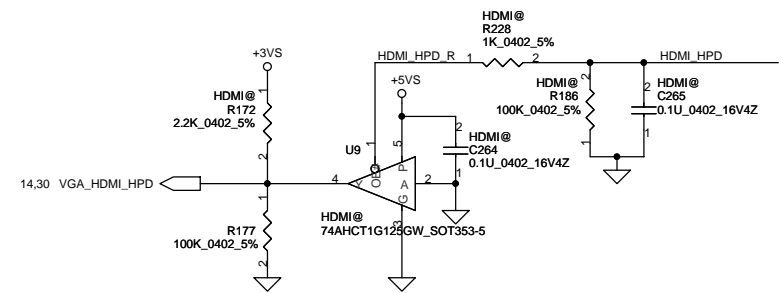
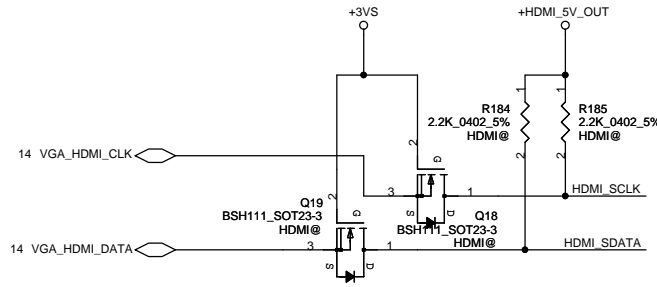
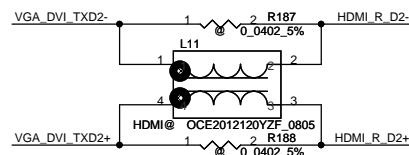
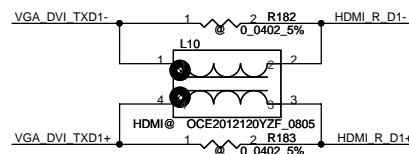
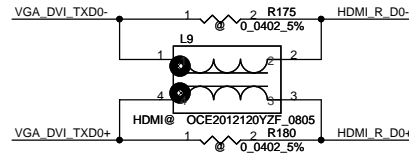
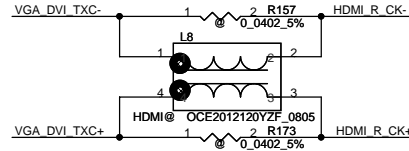
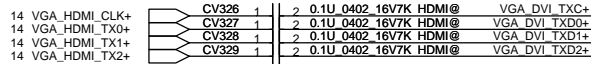
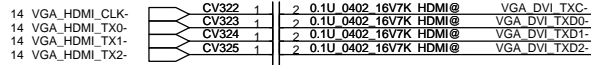
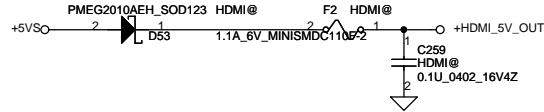
LCD/PANEL BD. Conn.



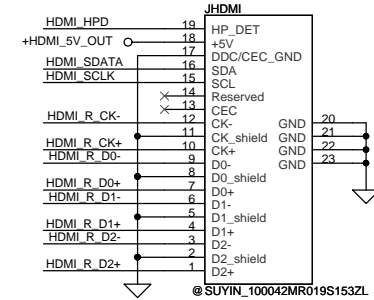
CRT CONNECTOR



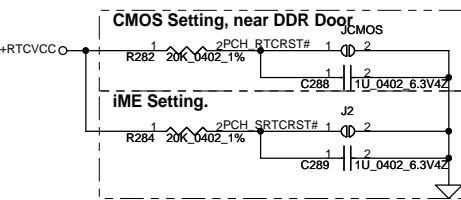
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HDMI Connector



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Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
--------------	---

HDA_SYNC

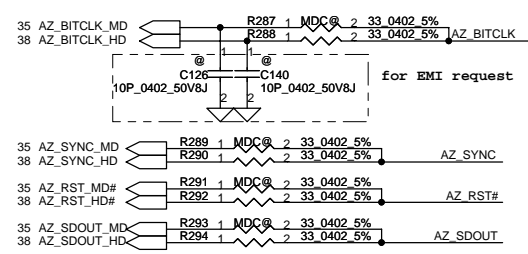
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V

HDA_SDO

This signal has a weak internal pull down.
This signal can't PU

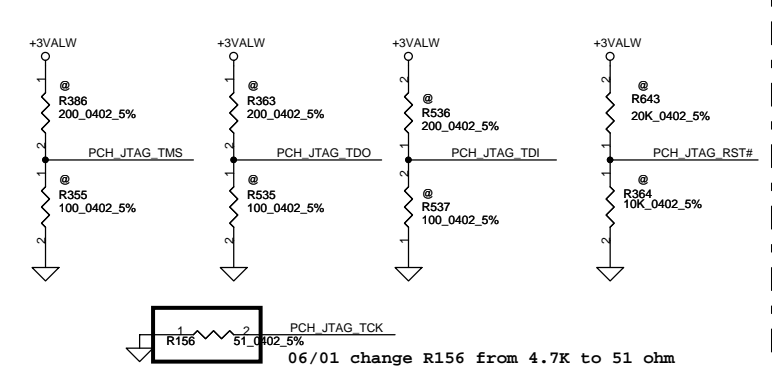
Flash Descriptor Security Override

HDA_DOCK_EN#	Low = Enabled High = Disabled *
--------------	------------------------------------

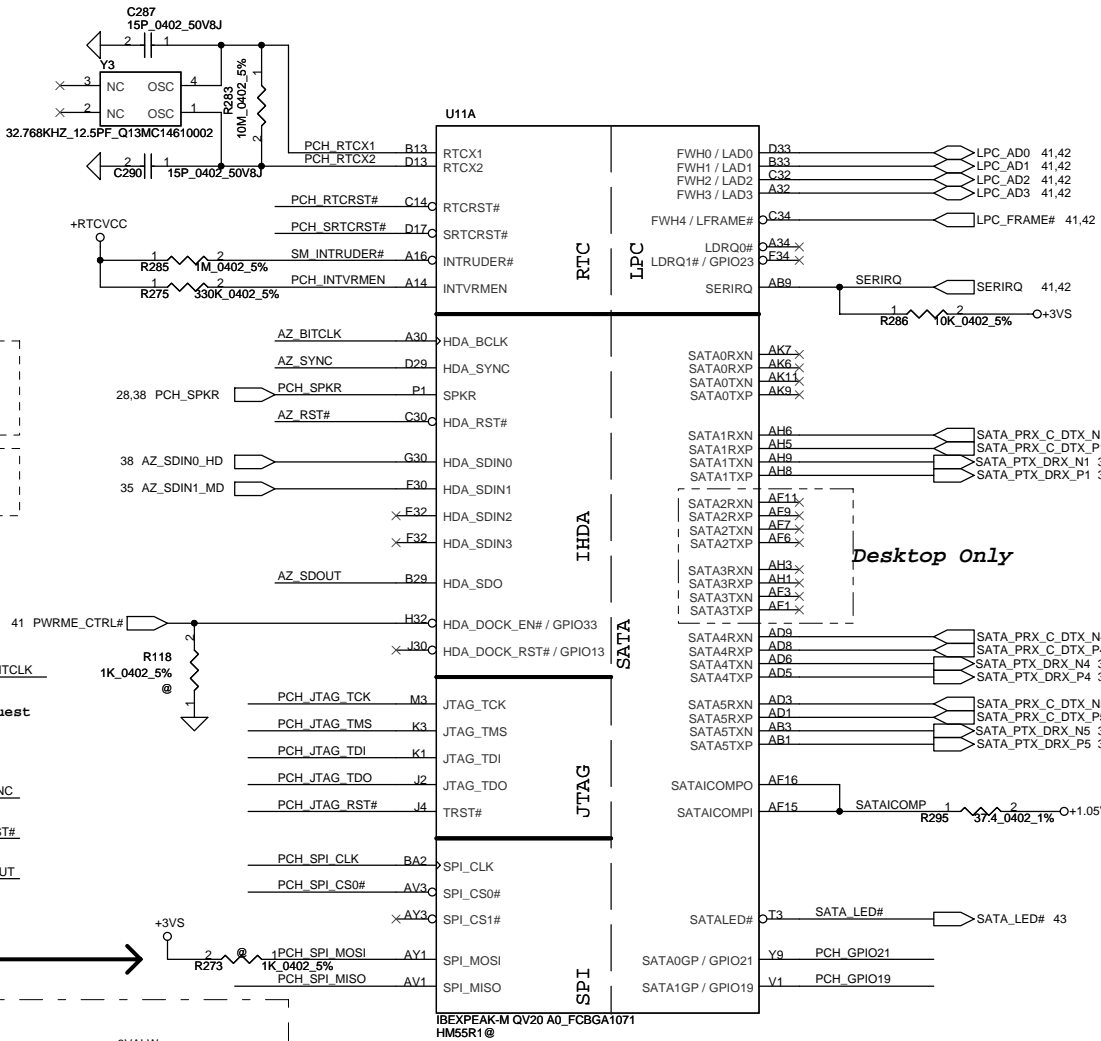


ITPM Enabled Internal: Pull down 20k

SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--



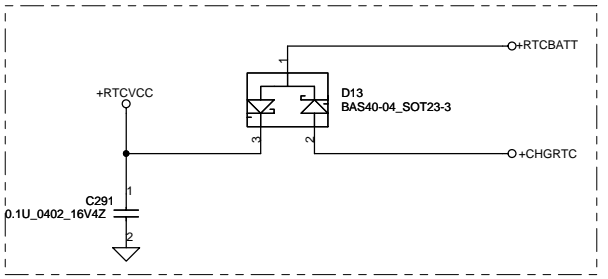
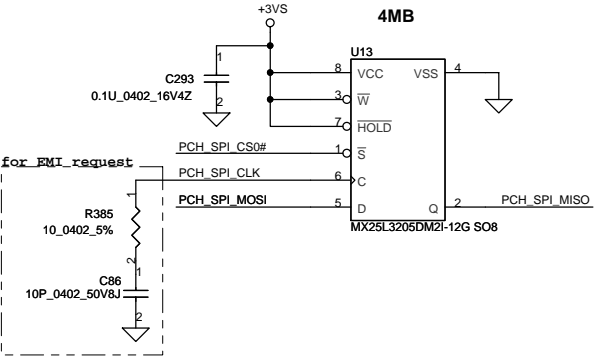
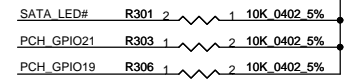
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	No Install	100ohm	No Install	No Install
PCH_JTAG_TCK	R156	No Install	200ohm	No Install	No Install
PCH_JTAG_RST#	R643	No Install	20Kohm	No Install	No Install



1ST HDD

SATA ODD

eSATA



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For LAN

37 PCIE_PRX_C_LANTX_N1
37 PCIE_PRX_C_LANTX_P1
37 PCIE_PTX_C_LANRX_N1
37 PCIE_PTX_C_LANRX_P1

For WLAN

36 PCIE_PRX_WLANTX_N2
36 PCIE_PRX_WLANTX_P2
36 PCIE_PTX_C_WLANRX_N2
36 PCIE_PTX_C_WLANRX_P2

LAN

37 CLK_LAN#
37 CLK_LAN#
37 CLKREQ_LAN#

WLAN

36 CLK_WLAN#
36 CLK_WLAN#
36 CLKREQ_WLAN#

PCH_GPIO20
PCH_GPIO25
PCH_GPIO26
PCH_GPIO44
PCH_GPIO56
PCH_GPIO20
PCH_GPIO25
PCH_GPIO26
PCH_GPIO44
PCH_GPIO56

U11B

NC

PCI-E*

SMBus

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M QV20 A0_FCBGA1071
HM55R1@

SMBALERT# / GPIO11
SMBCLK
SMBDATA
SML0ALERT# / GPIO60
SML0CLK
SML0DATA
SML1ALERT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GPIO75
CL_CLK1
CL_DATA1
CL_RST1#

CL_CLK1
CL_DATA1
CL_RST1#

PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P

CLKIN_DMI_N
CLKIN_DMI_P

CLKIN_BCLK_N
CLKIN_BCLK_P

CLKIN_DOT_96N
CLKIN_DOT_96P

CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P

REFCLK14IN

XTAL25_IN
XTAL25_OUT

XCLK_RCOMP

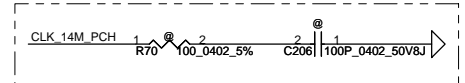
CLKOUTFLEX0 / GPIO64

CLKOUTFLEX1 / GPIO65

CLKOUTFLEX2 / GPIO66

CLKOUTFLEX3 / GPIO67

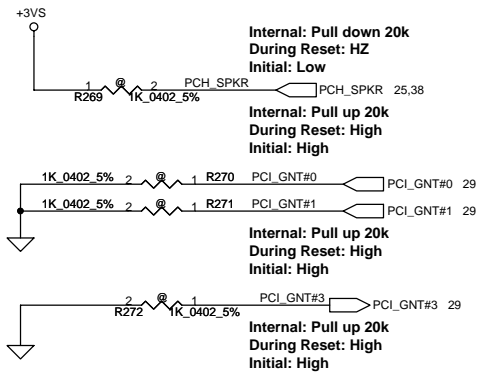
FROM CLK GEN FOR: 133/100/96/14.318 MHZ



PCH_SMLCLK0 2.2K 0402 5% 2 R237
PCH_SMLDATA0 2.2K 0402 5% 2 R238
PCH_GPIO60 10K 0402 5% 2 R239
PCH_GPIO74 10K 0402 5% 2 R240
EC_LID_OUT# 10K 0402 5% 2 R241

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PCH Strap Pin



NO REBOOT Strap

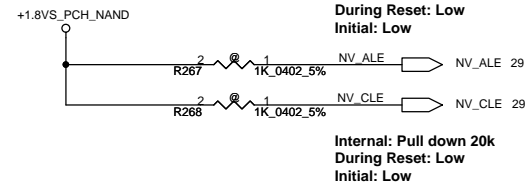
PCH_SPKR	Low= Disable High= Enable
----------	------------------------------

Boot BIOS Strap

PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap

PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable
-----------	--

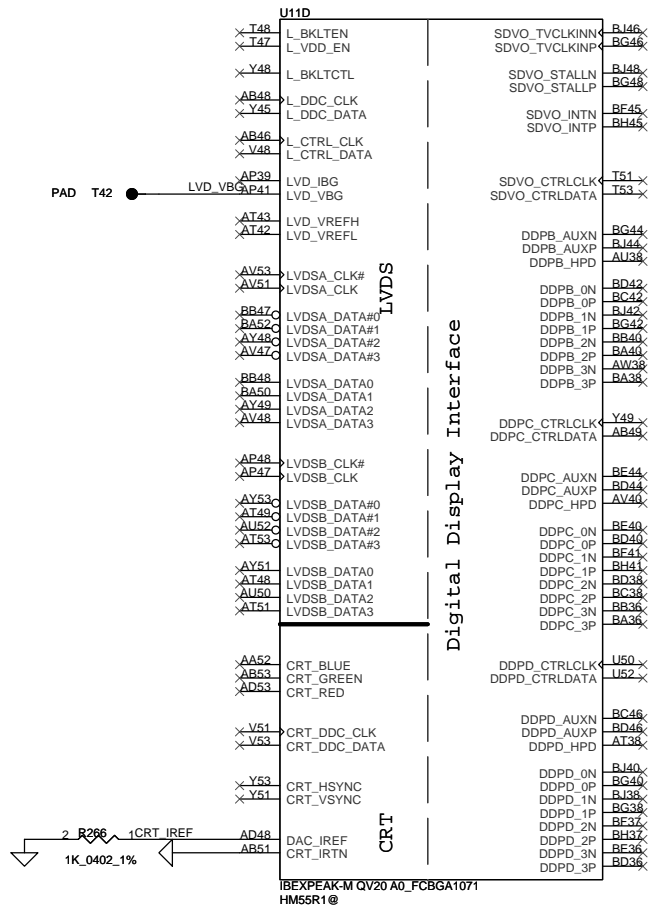


Danbury Technology Enabled

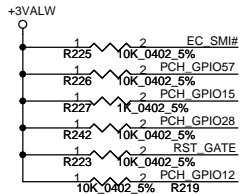
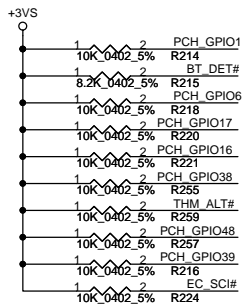
NV_ALE	High = Enabled Low = Disabled (Default)
--------	--

DMI Termination Voltage

NV_CLE	Low= Set to Vss (Default) High= Set to Vcc
--------	---



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GPIO8 Not pull down

Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

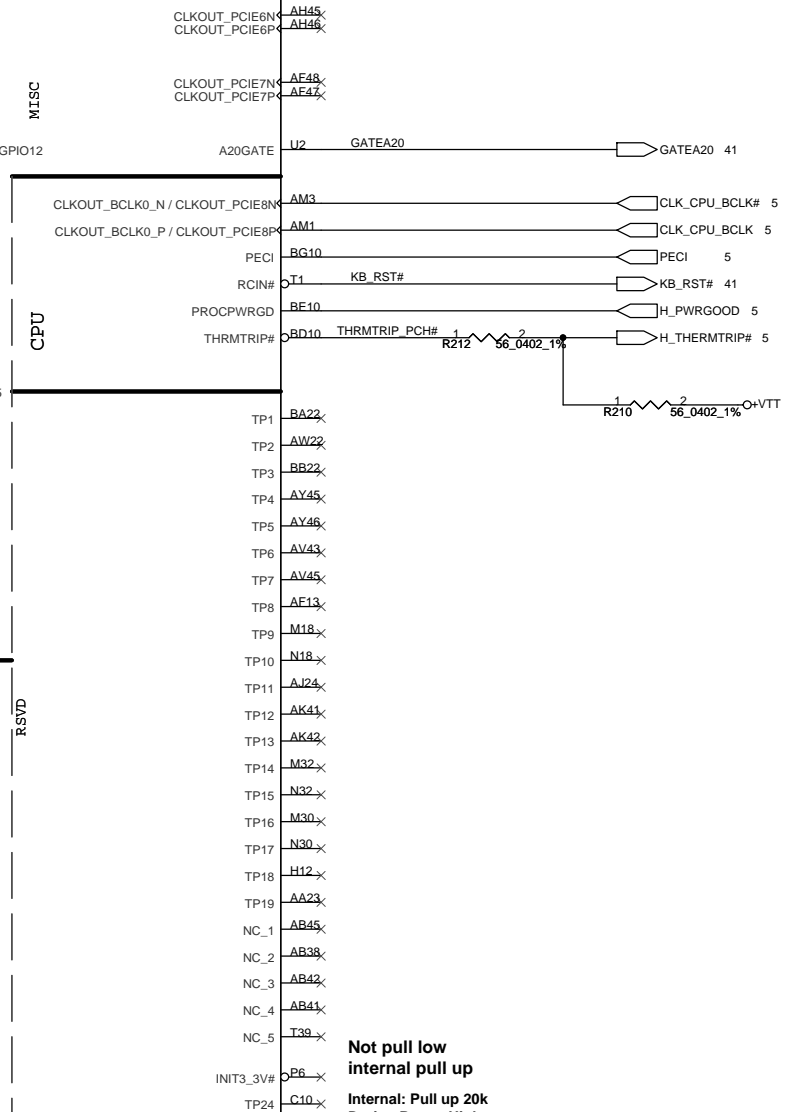
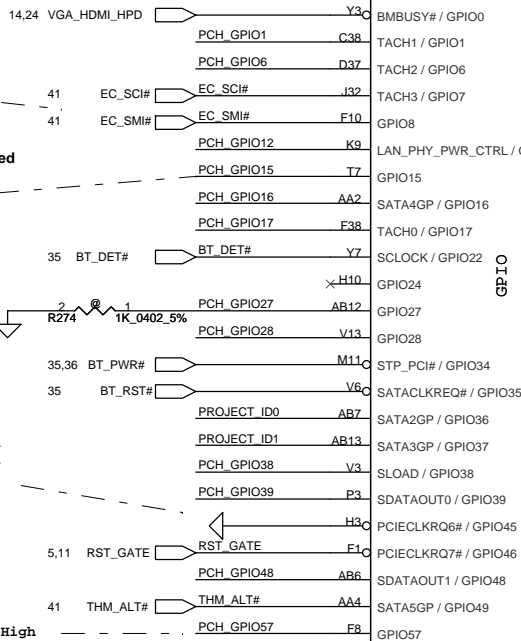
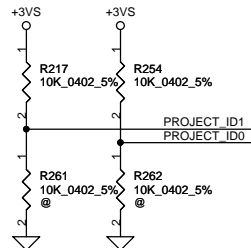
On-Die PLL VR	
PCH_GPIO27	High = Enabled (Default) Low = Disabled

GPIO39:
CIR_EN# : Pull-High
for non-support CIR

GPIO45:
LVDS_SEL : GND for
Dual-Channel Panel

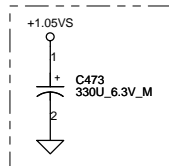
GPIO57:
OPTIMUS_EN# : Pull-High
for non-support OPTIMUS

PROJECT_ID			
Name	ID1	ID0	
NBQAA 11.6/13.3"	L	L	
NBQAA 14"	L	H	
NWQAA 16"	H	L	
*NALAA 17.3"	H	H	

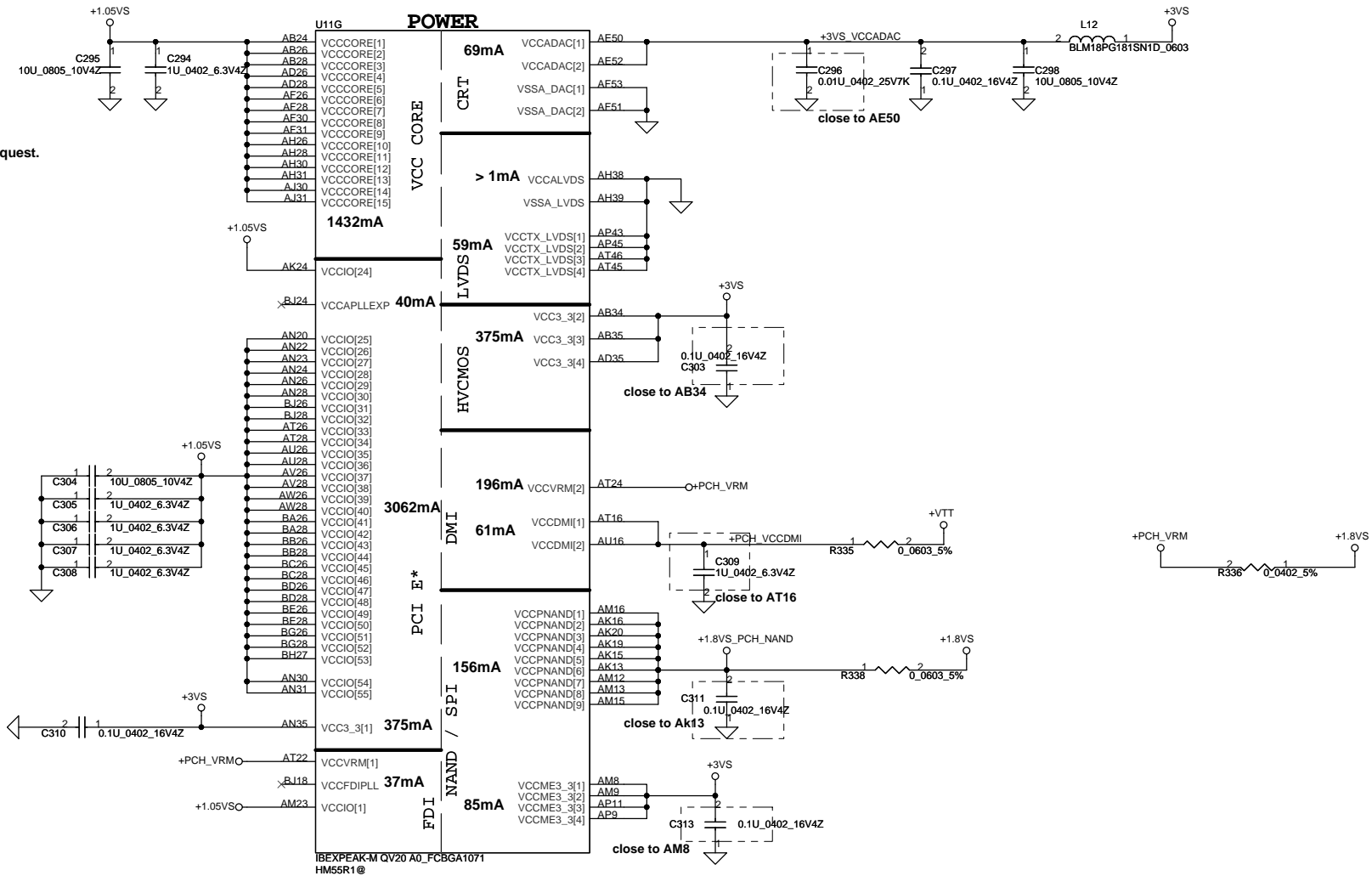


Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High

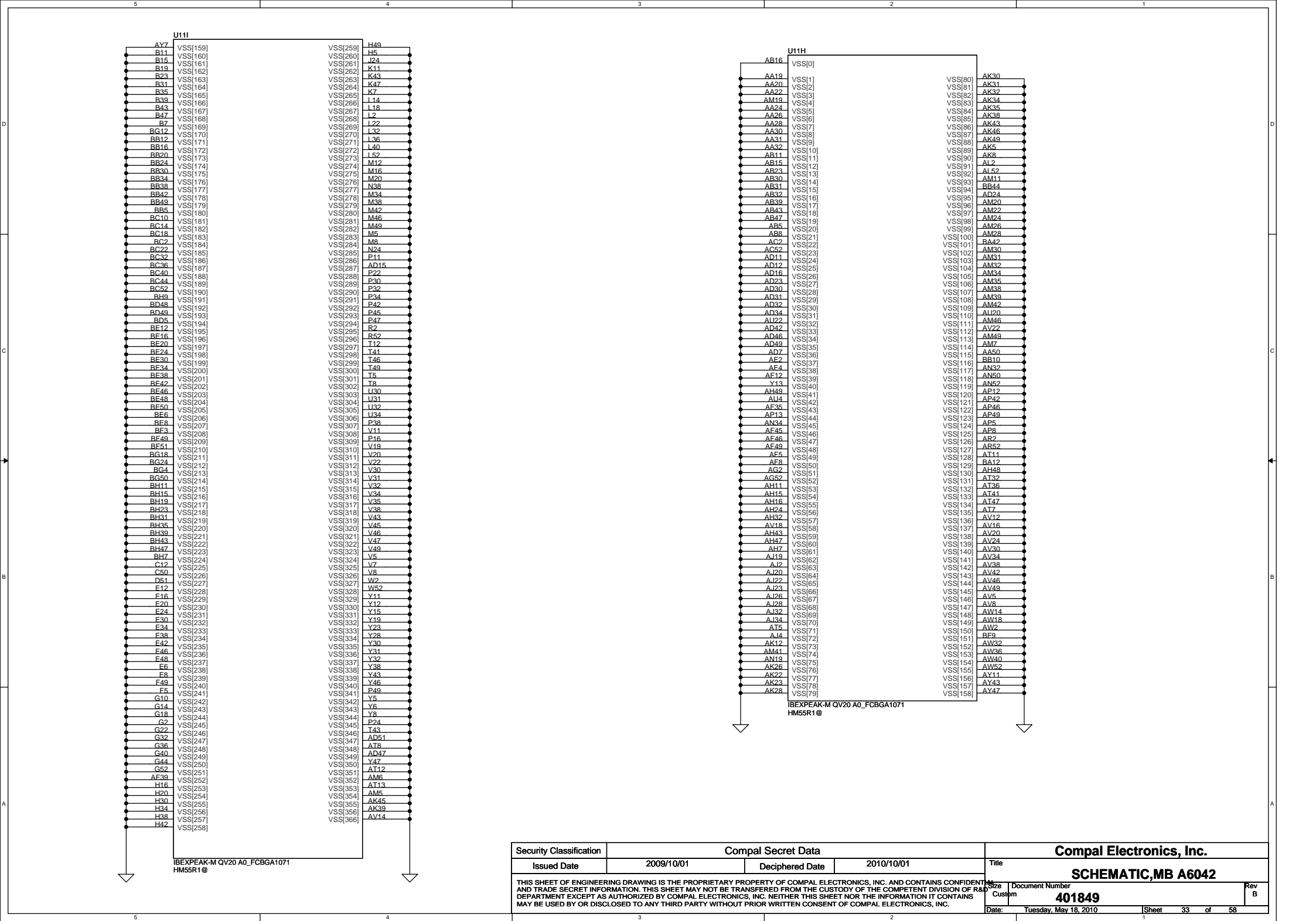
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12/16: Add for power team request.

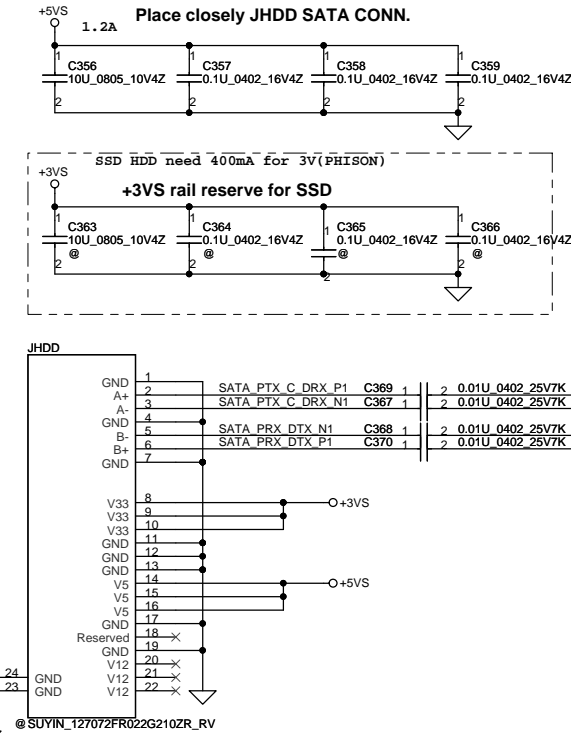


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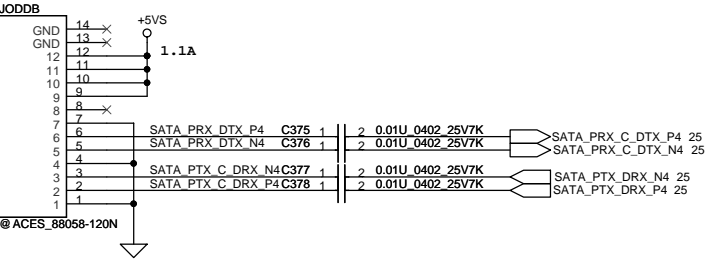


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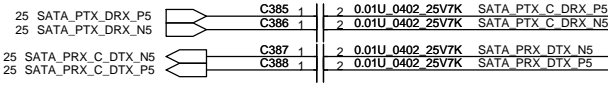
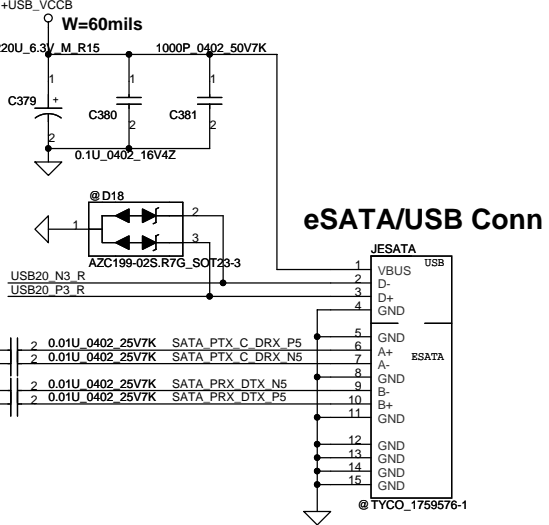
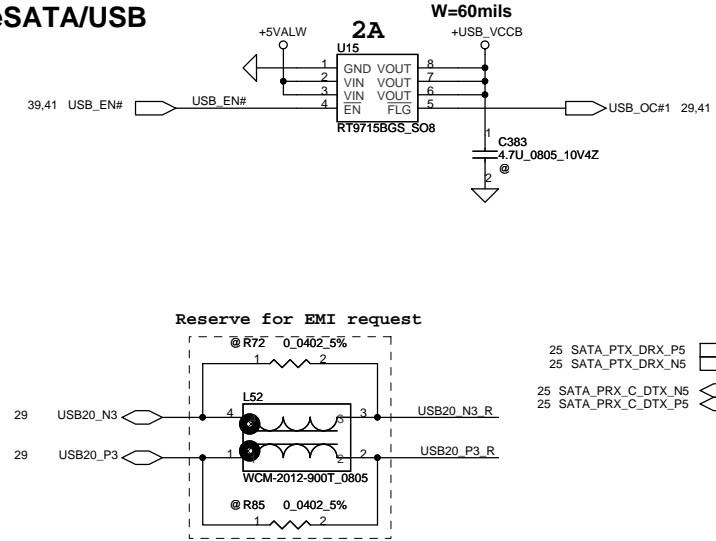
SATA HDD Conn.



SATA ODD Conn

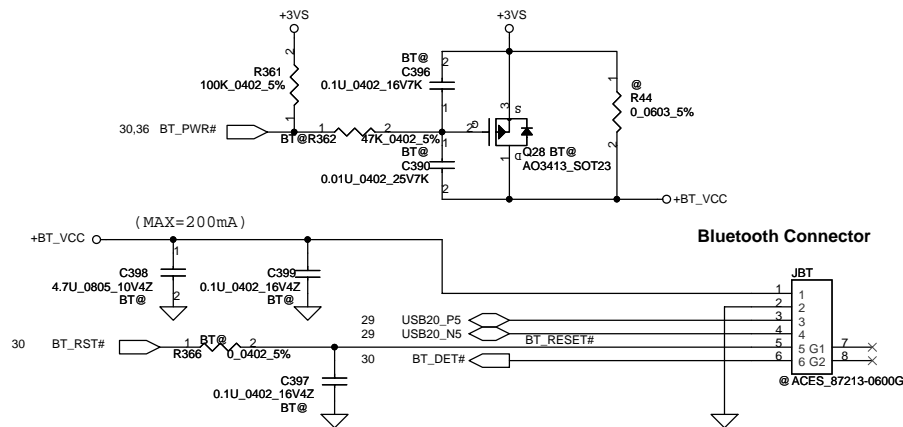


eSATA/USB

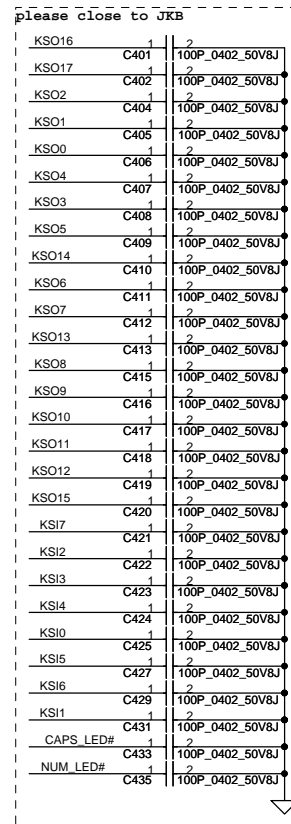
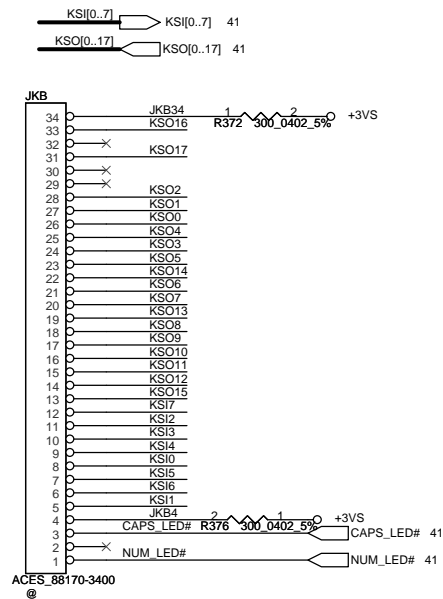


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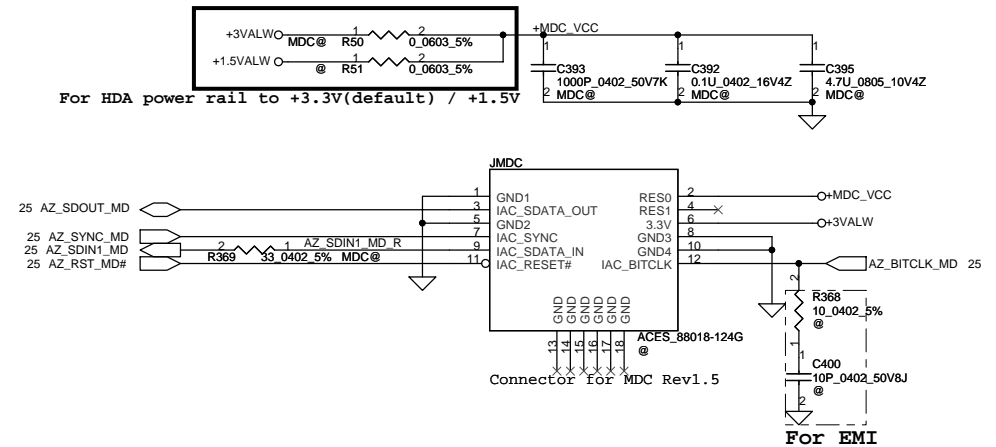
Bluetooth Interface



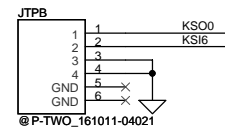
KEYBOARD
CONN.



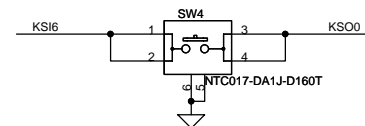
MDC 1.5 Conn.



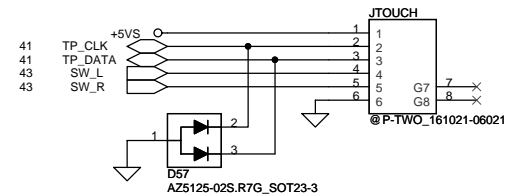
TP On&Off BTN Conn.



TP On&Off BTN On M/B

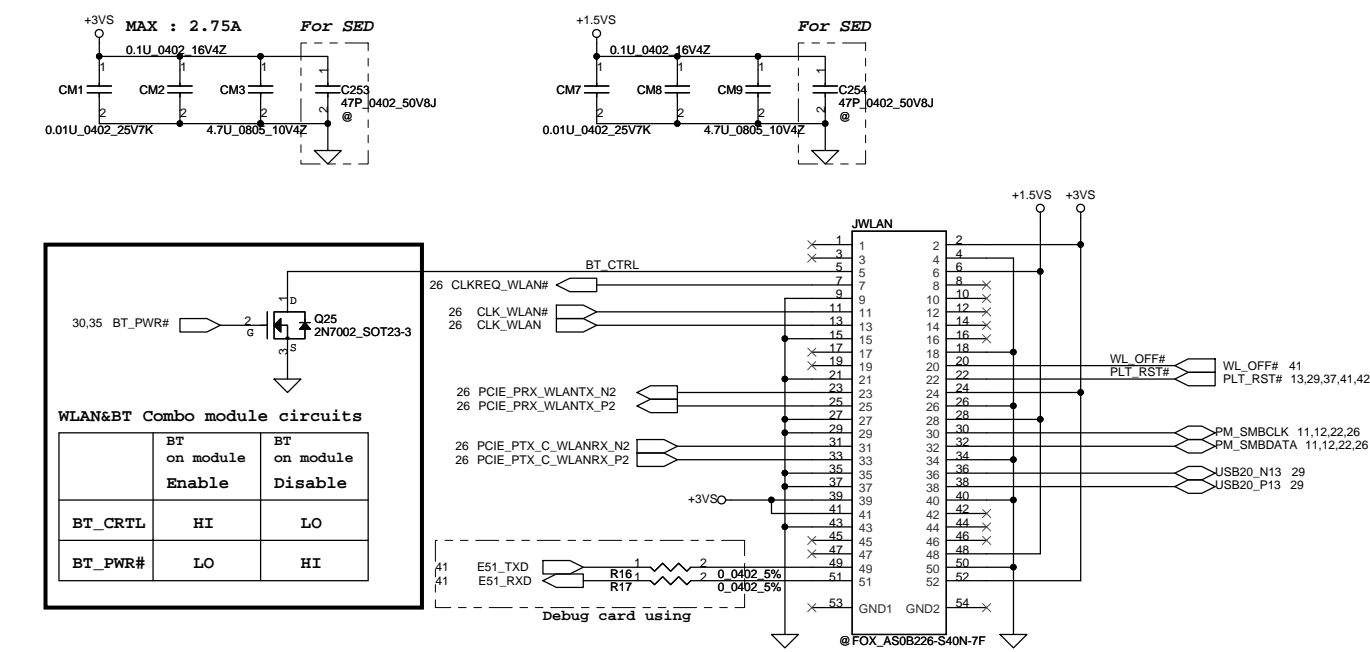


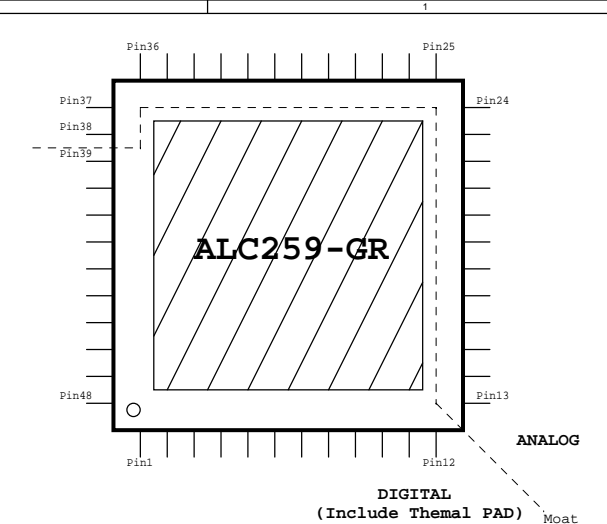
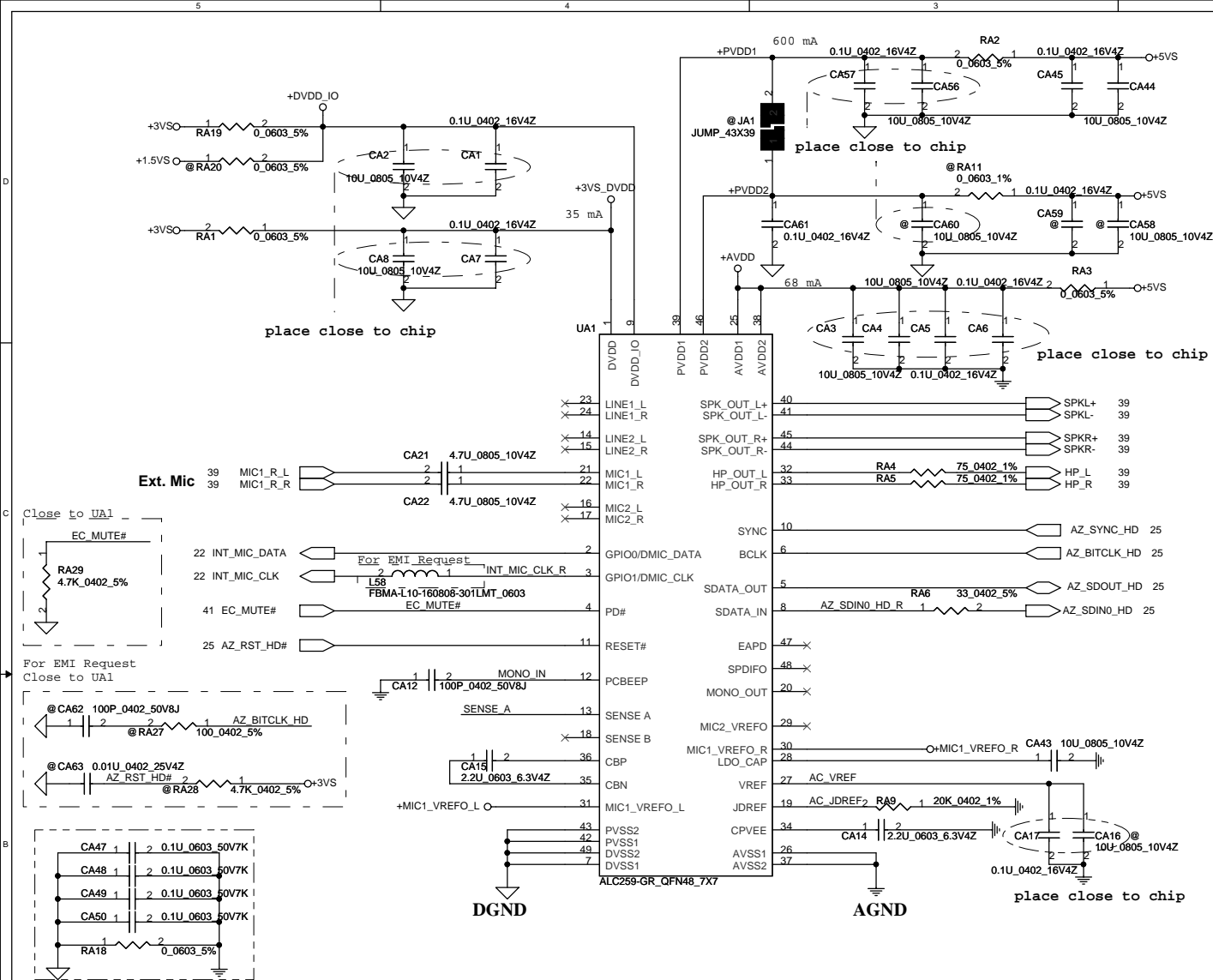
Touch PAD Connector



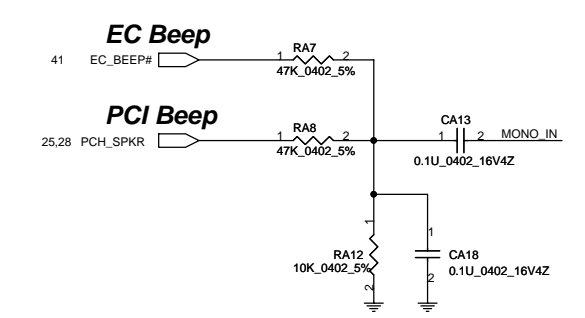
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PCIe Mini Card-WLAN

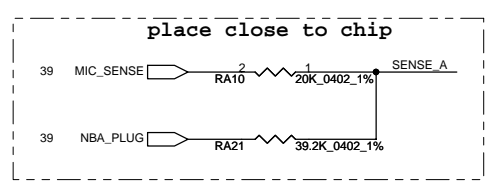




Beep sound

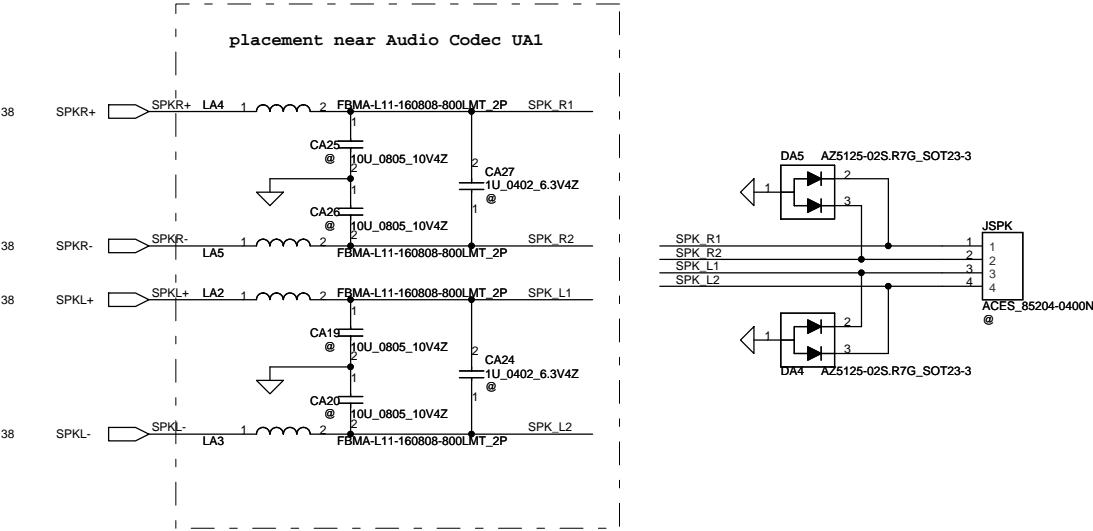


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

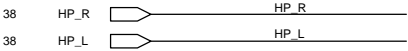


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					401849
				Date:	Tuesday, May 18, 2010
				Sheet	38 of 58

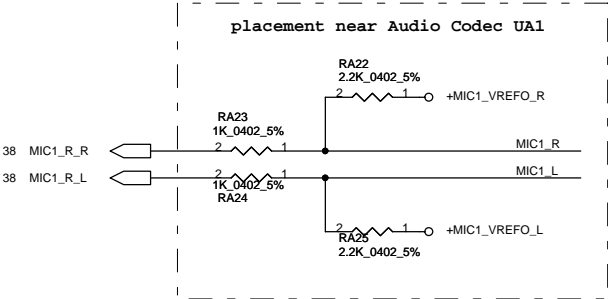
Speaker Connector



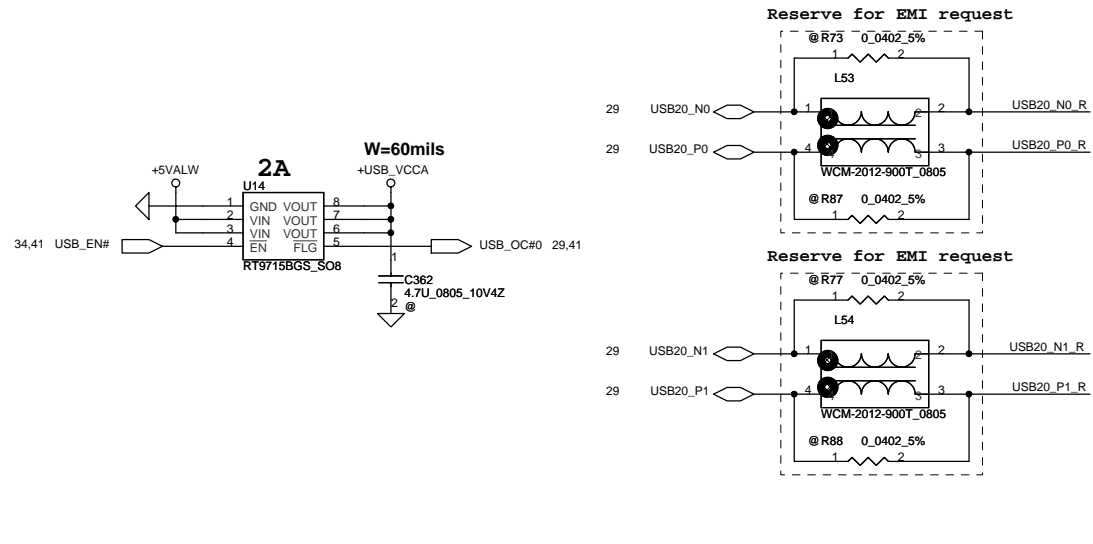
HeadPhone/LINE Out JACK



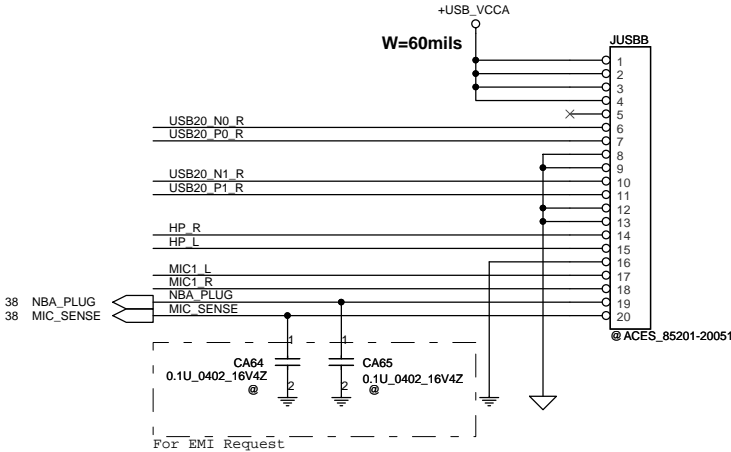
Ext.MIC/LINE IN JACK



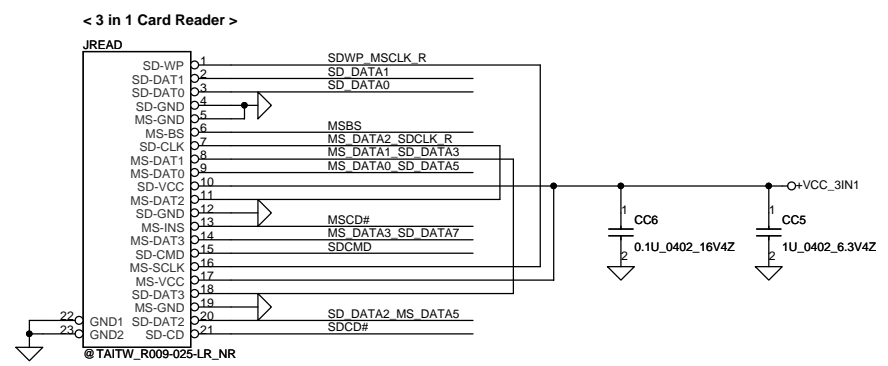
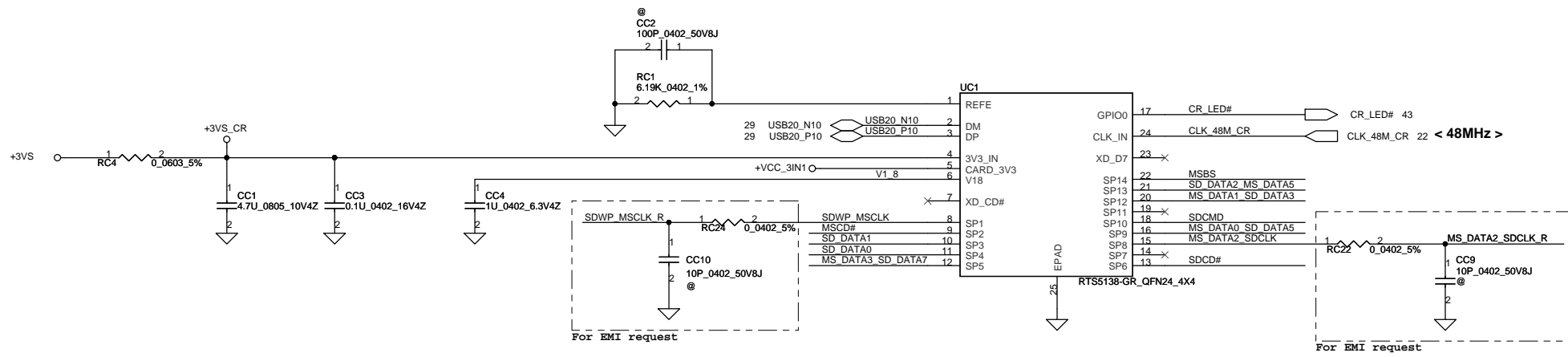
USB Board



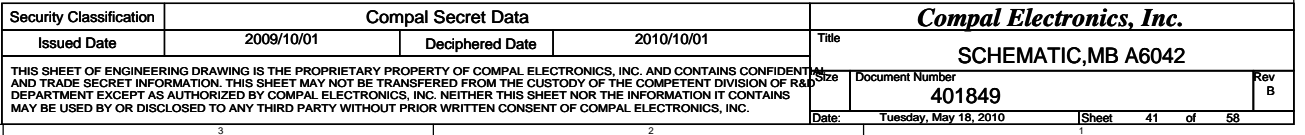
Audio & USB Sub-Board Conn.



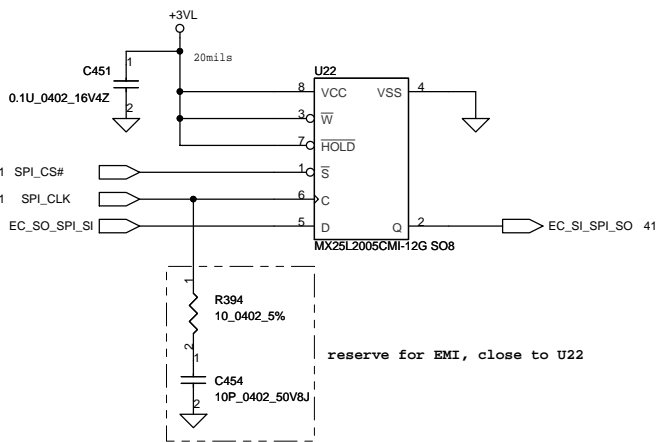
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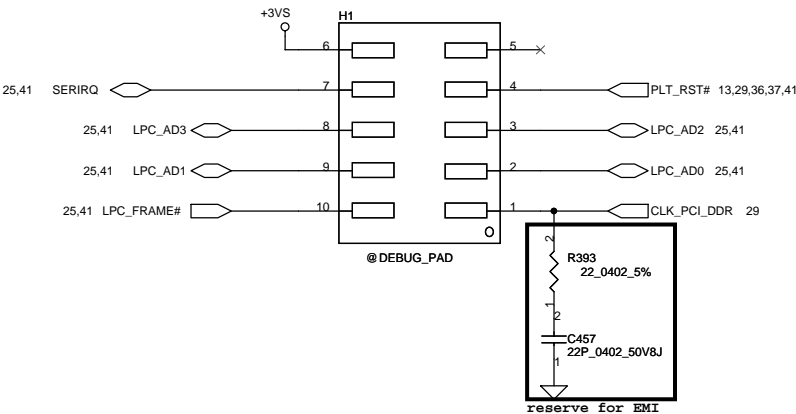


SPI Flash (256KB)



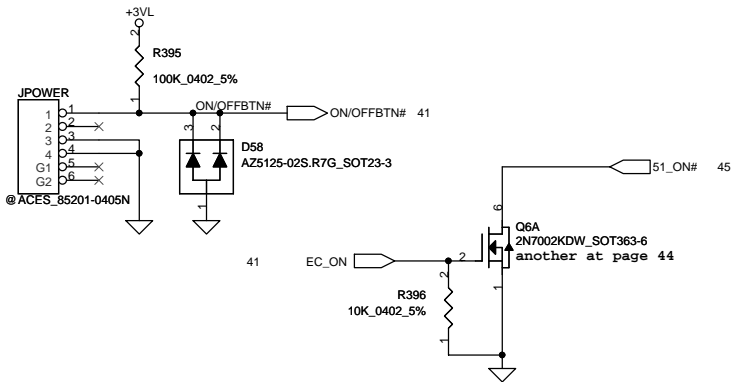
LPC Debug Port

Please place the PAD under DDR DIMM.

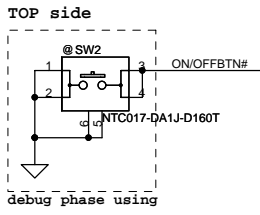


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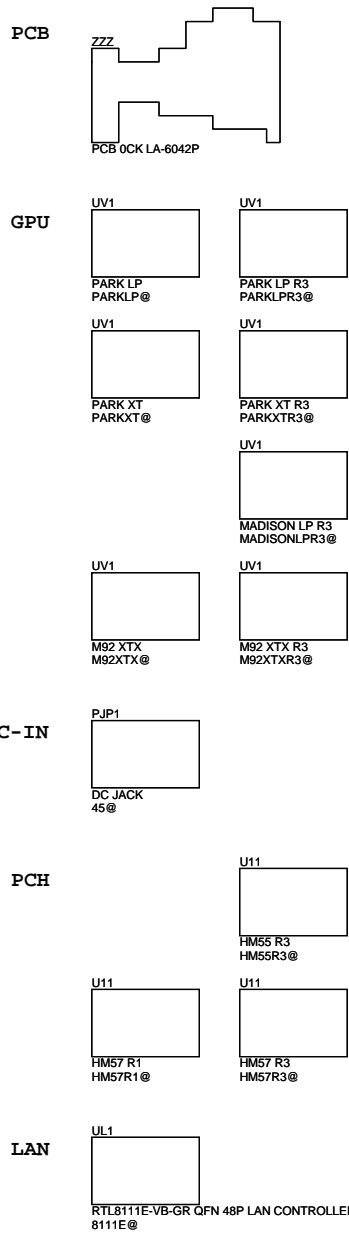
Power Button Circuit



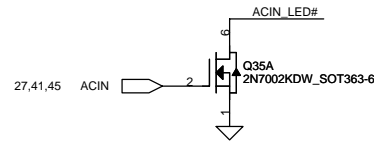
Debug Button



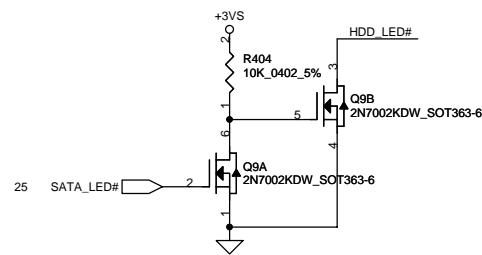
ISPD



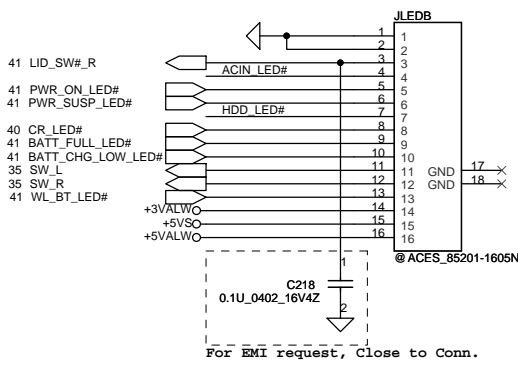
DC-IN LED Control Circuit



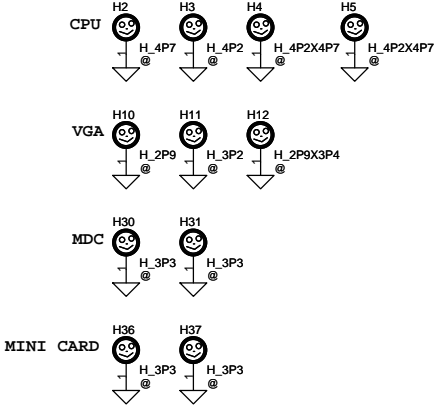
HDD LED Control Circuit



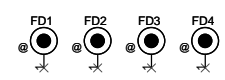
LED/B Conn.



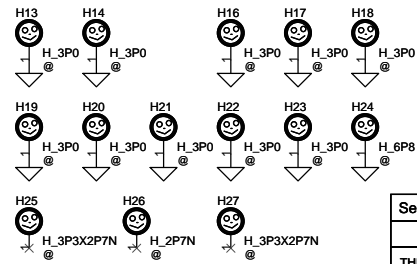
Screw Hole



PCB Fedical Mark PAD

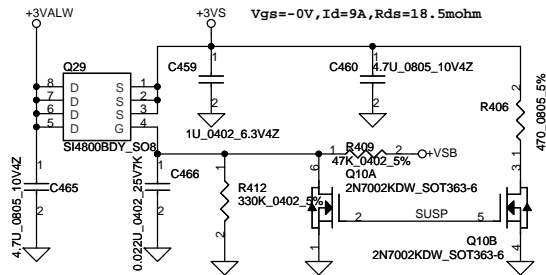


Others

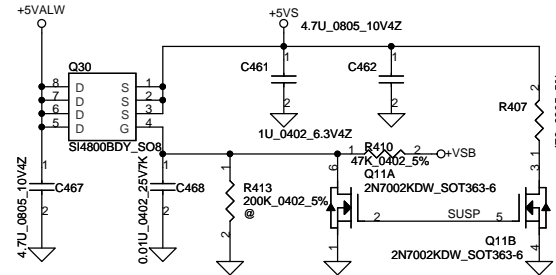


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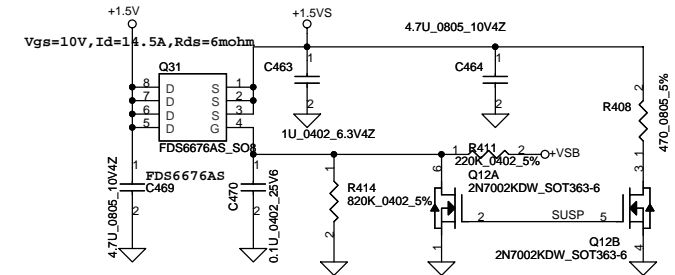
+3VALW TO +3VS



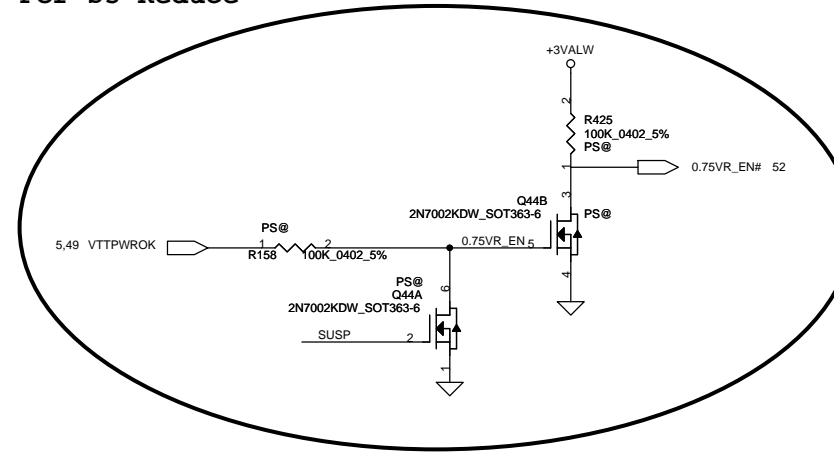
+5VALW TO +5VS



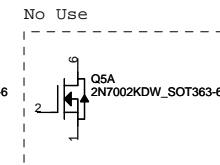
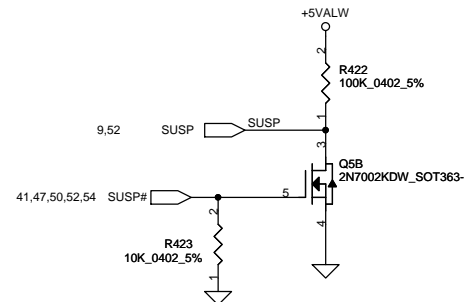
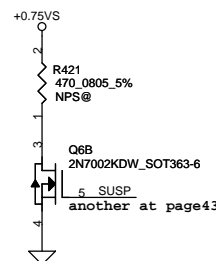
+1.5V to +1.5VS



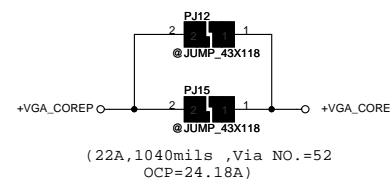
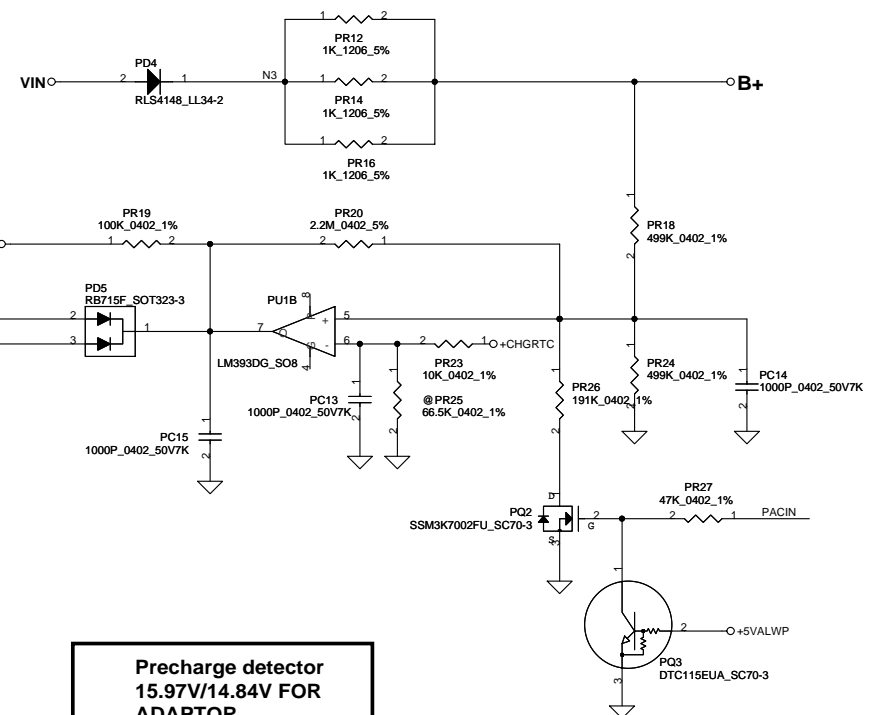
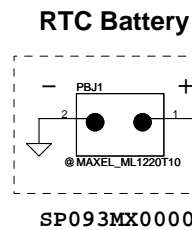
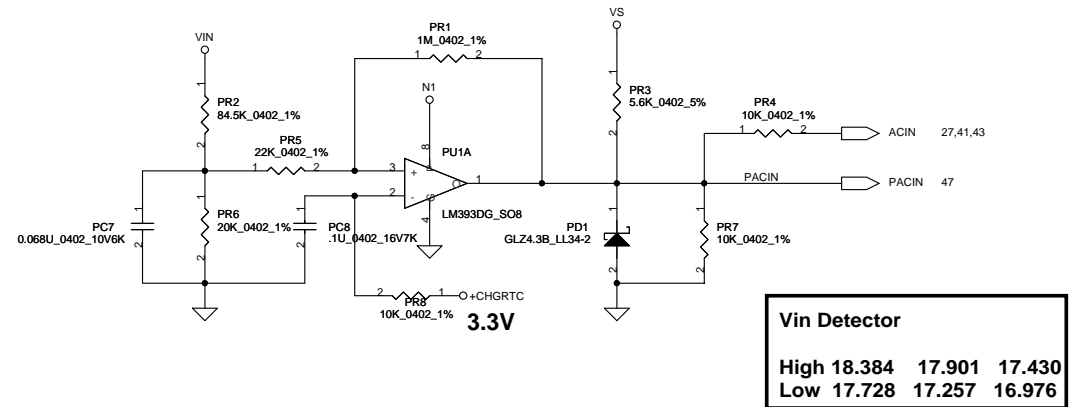
For S3 Reduce



For S3 Reduce

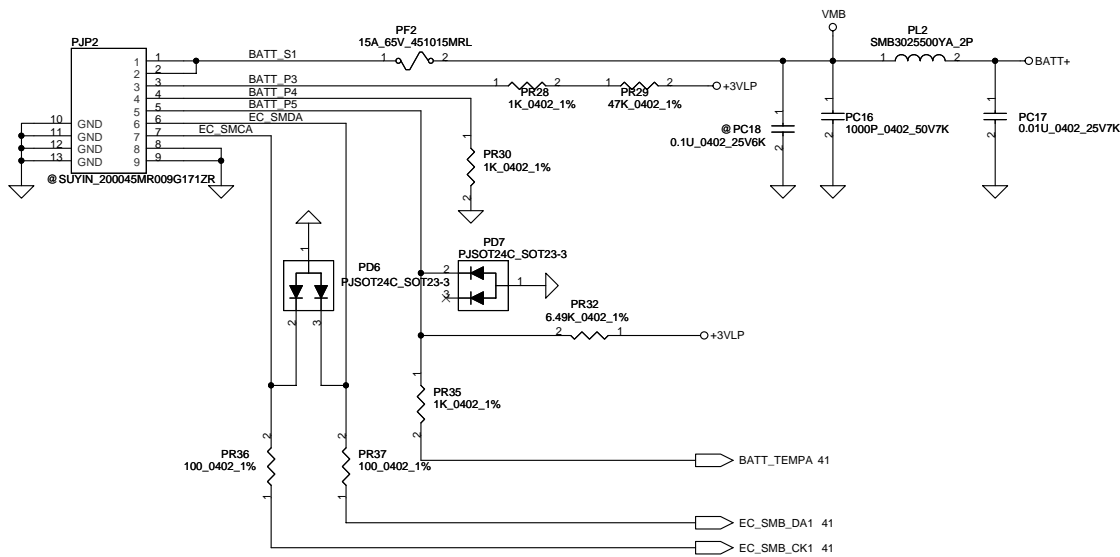


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Precharge detector 15.97V/14.84V FOR ADAPTOR

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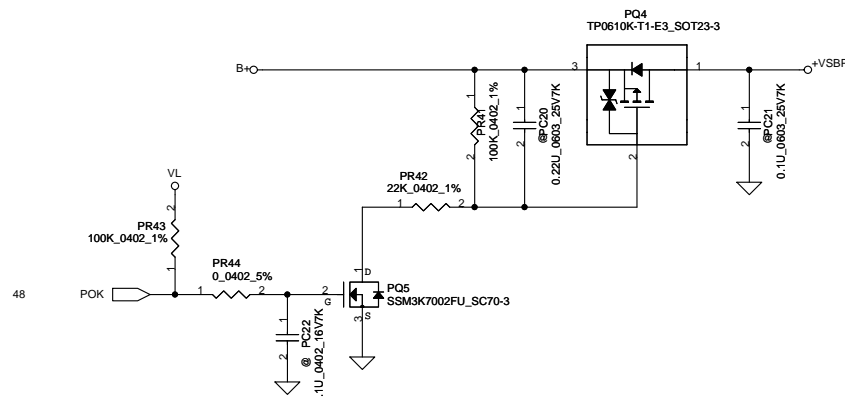
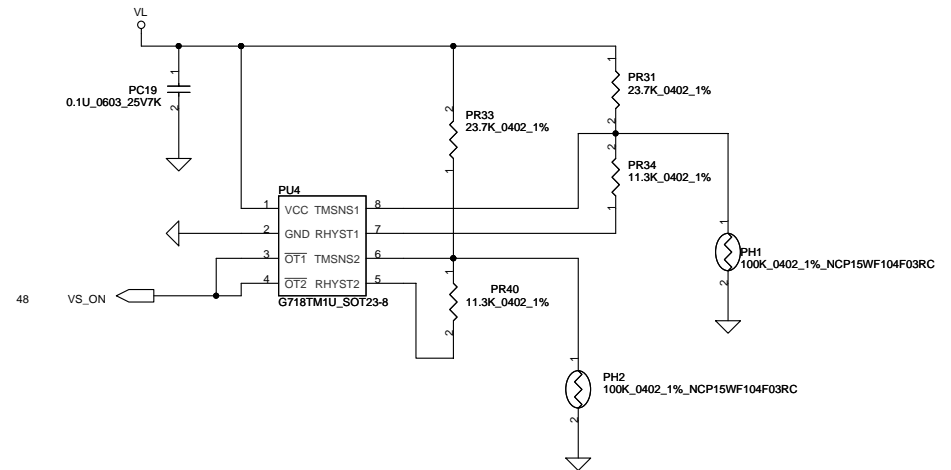


PH1 under CPU botten side :

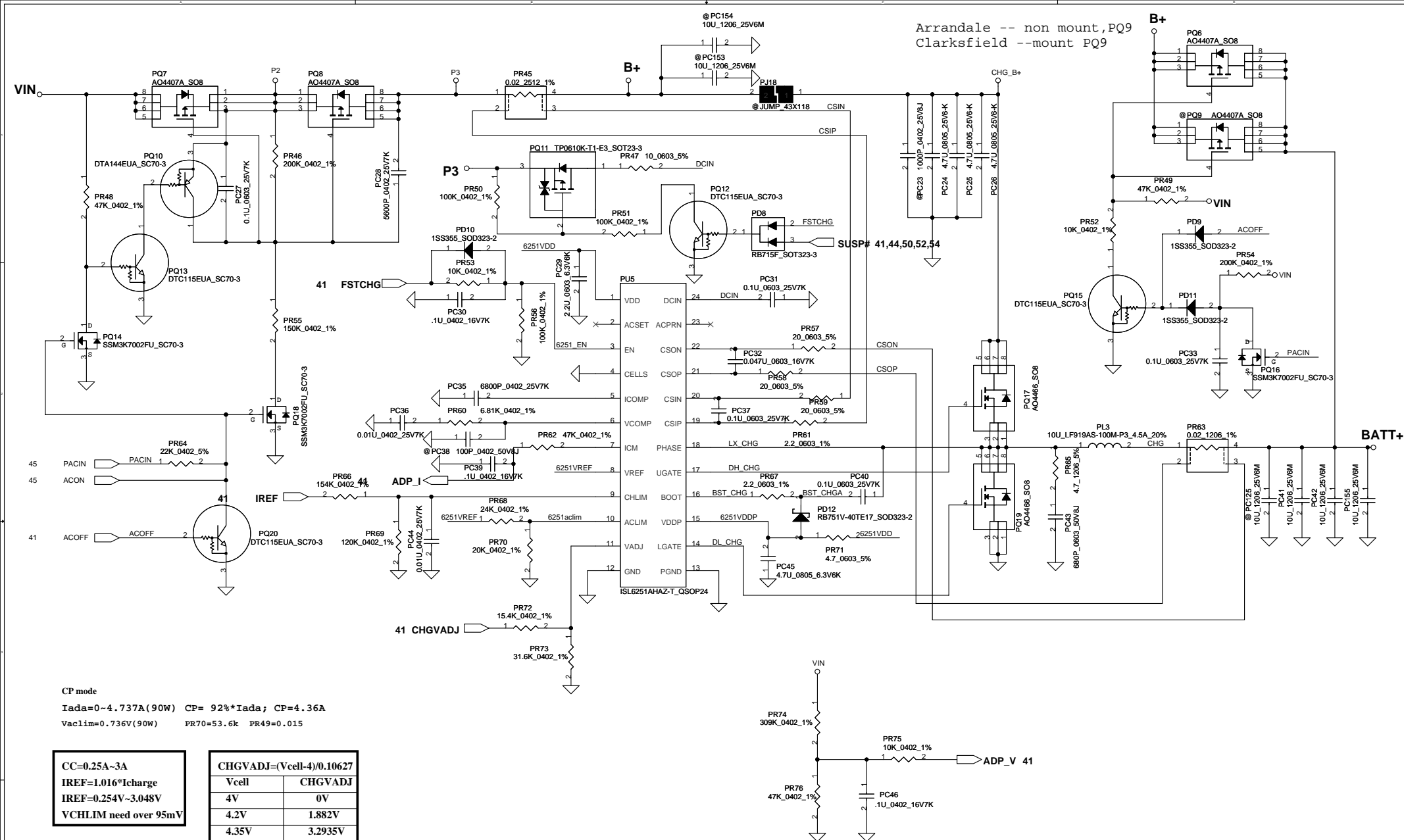
CPU thermal protection at 90 degree C
Recovery at 56 degree C

PH2 near main Battery CONN :

BAT. thermal protection at 90 degree C
Recovery at 56 degree C

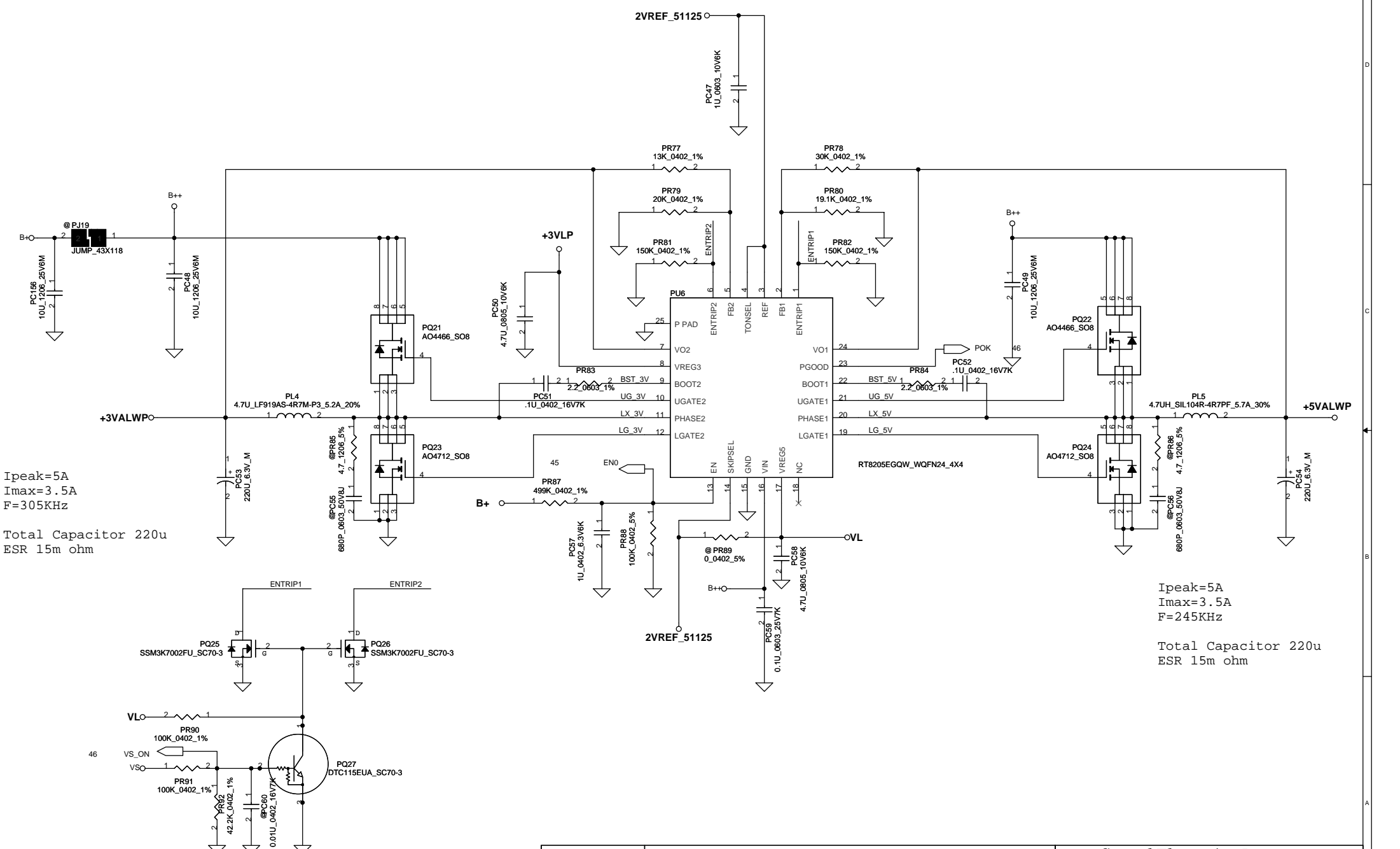


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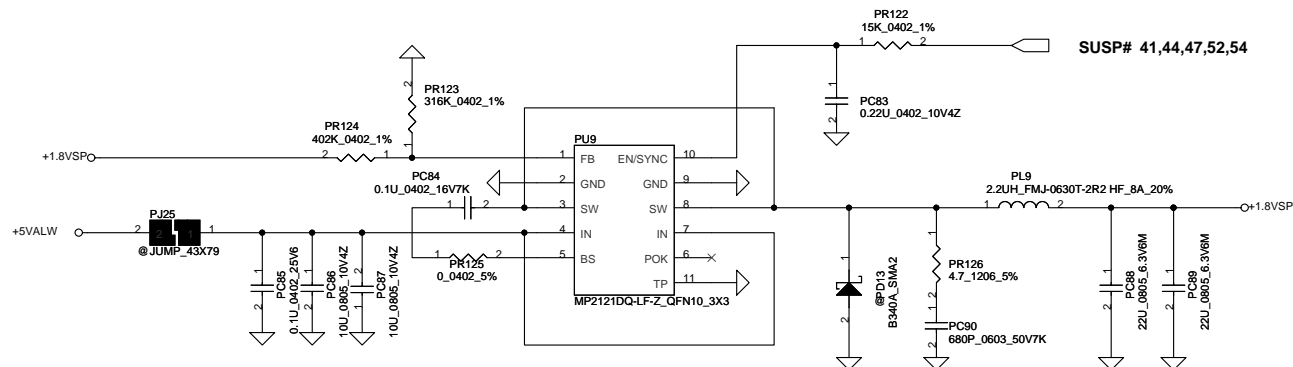
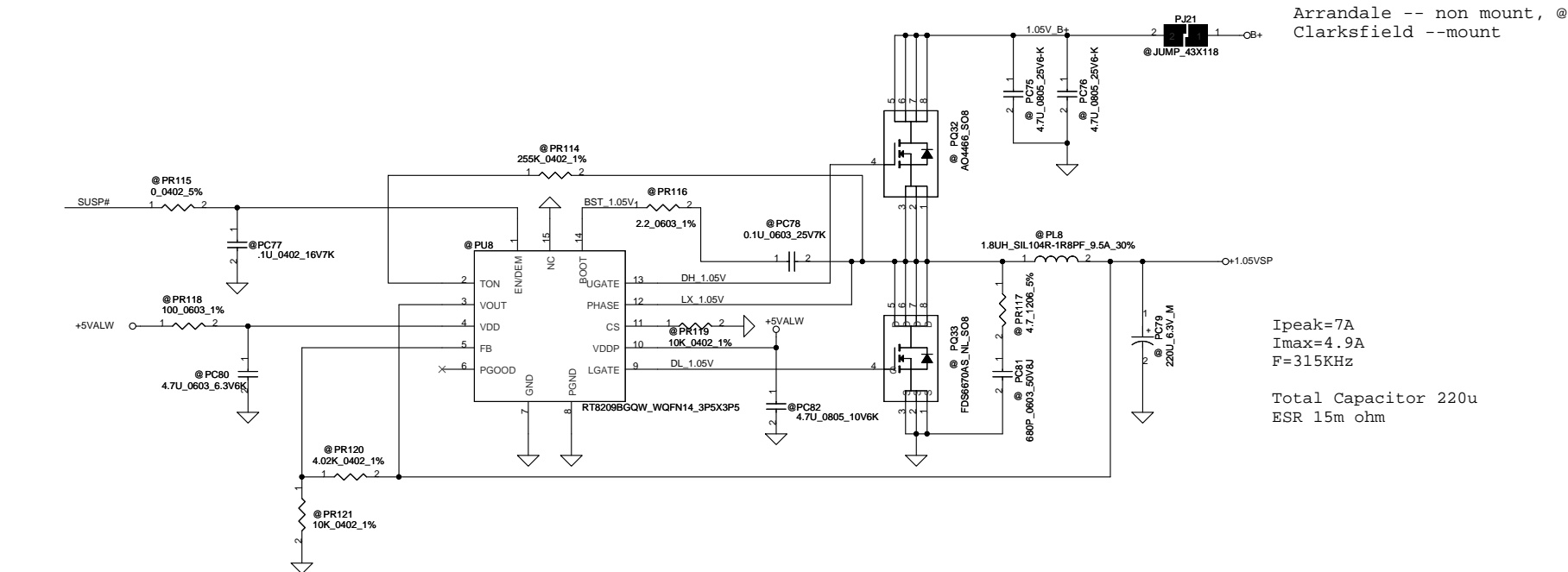


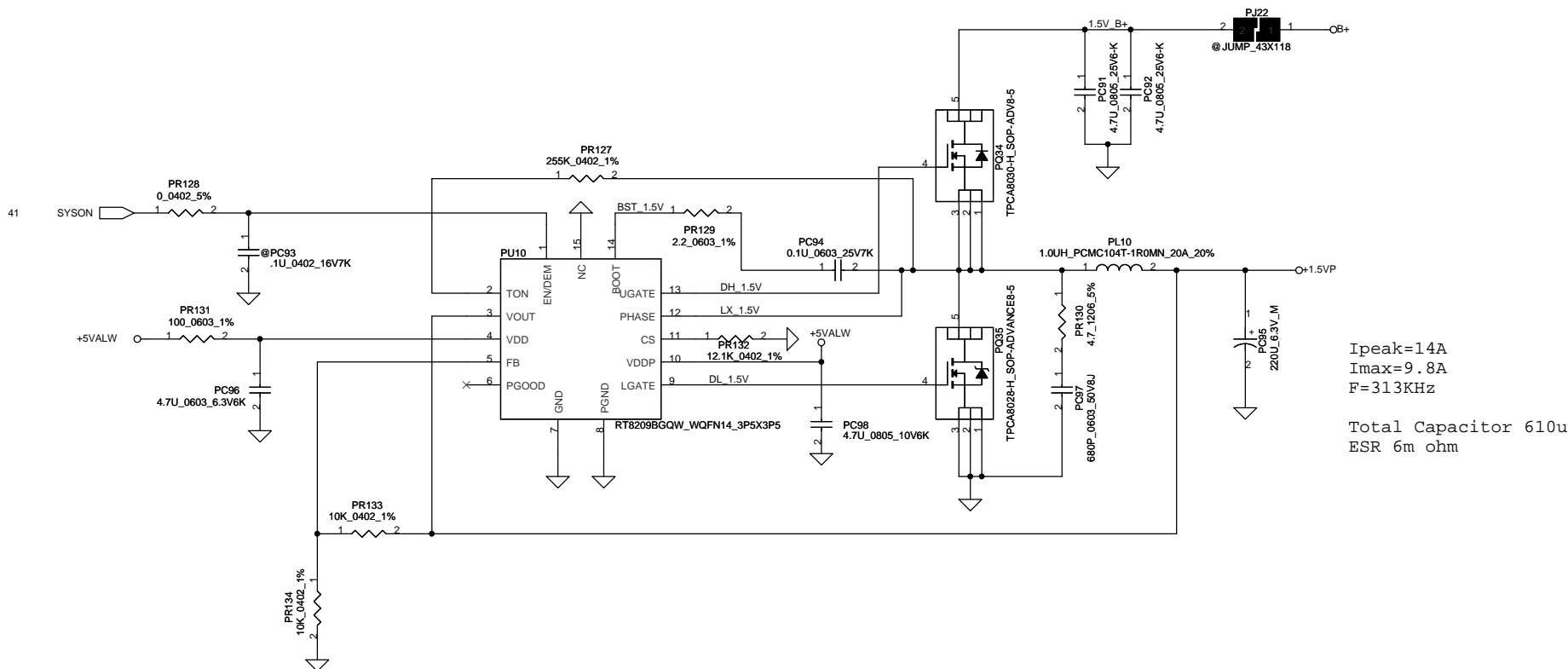
Ipeak=5A
 Imax=3.5A
 F=305KHz
 Total Capacitor 220u
 ESR 15m ohm

Ipeak=5A
 Imax=3.5A
 F=245KHz
 Total Capacitor 220u
 ESR 15m ohm

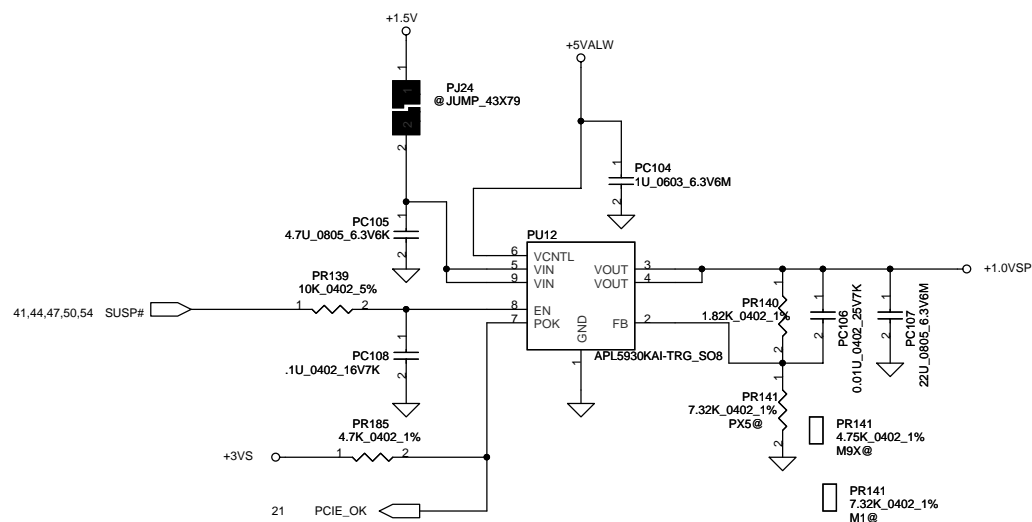
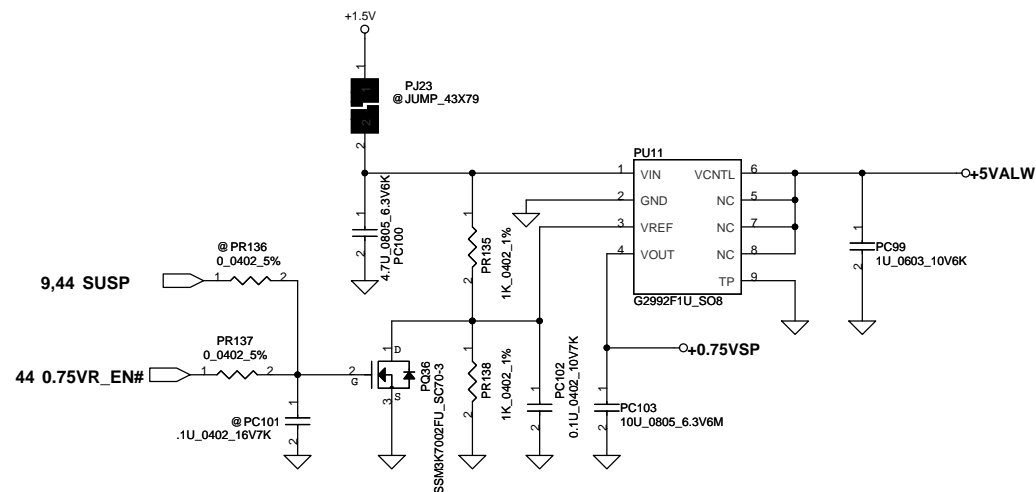


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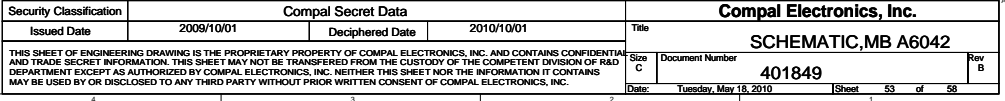


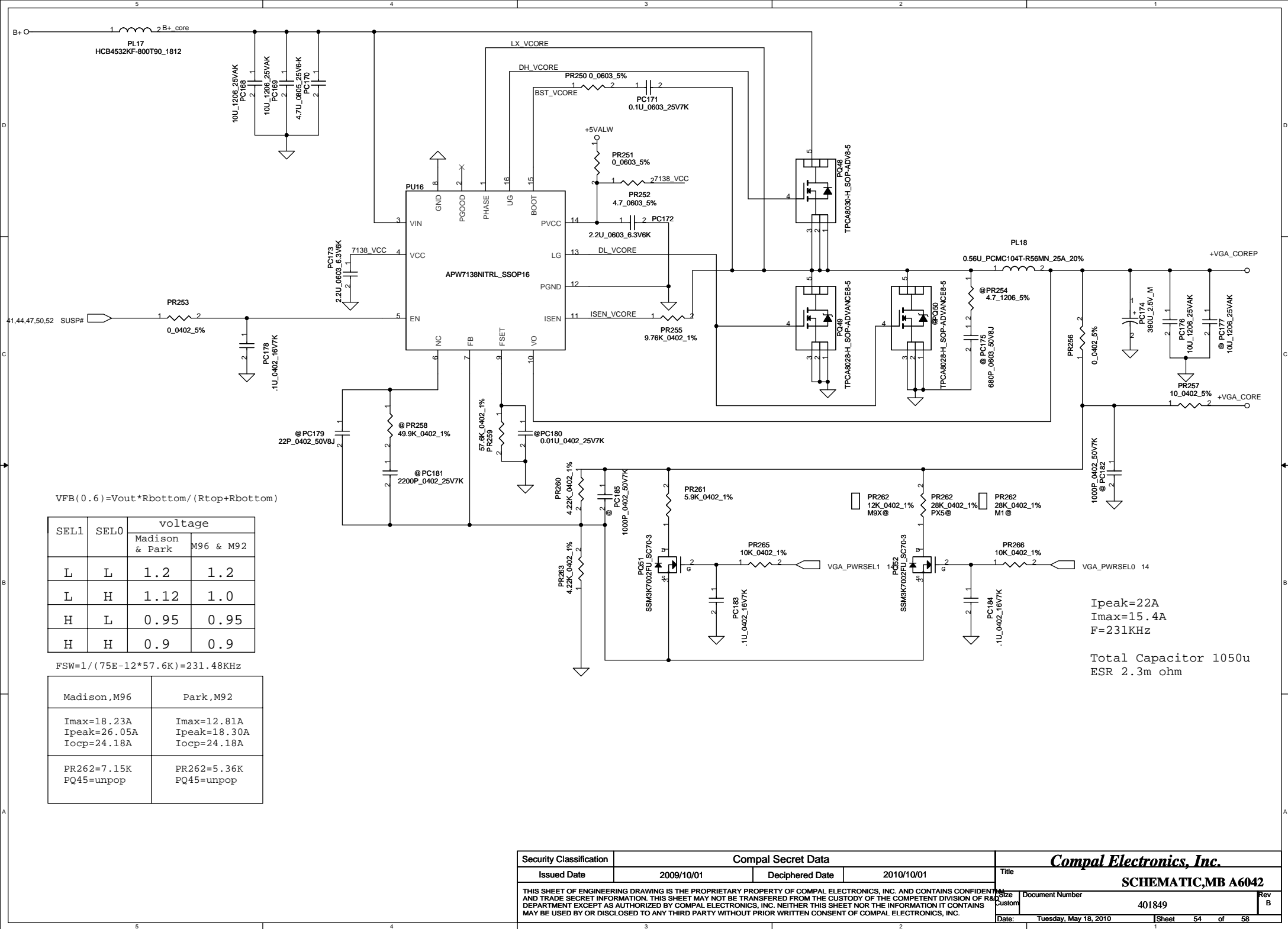


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NO DATE	PAGE	MODIFICATION LIST	PURPOSE
2009/10/20	45-56	Release	
2009/11/17	50	Change PL9 to SH00000FD10	BOM modify
2009/11/17	54	Change PC177 to unmount	circuit modify
2009/11/17	53	Change PH4 to SL200001000	circuit modify
2009/11/17	47,51	Change PC24,PC25,PC26,PC91,PC92 to SE000006R80	circuit modify
2009/12/15	48	Change PR92 to 42.2K ohm	circuit modify
2009/12/15	49	Change PR95 to 2.43K ohm,PR101,PC71,PC72 to unmount PR98 to 6.49K ohm	circuit modify
2009/12/15	51	Change PR132 to 6.19K ohm	circuit modify
2009/12/15	52	Add PR185	HW request
2009/12/15	54	Change PR258,PC179,PC181 to unmount	circuit modify
2009/12/25	48	Change PL4,PL5 to SH000006380(4 mm high)	Thermal request
2009/12/28	53	Change PC111,PC114 to 68U	DFB request
2010/01/05	46	Change PR31,PR33 to 19.6K ohm,PR34 to 8.66K ohm PR40 to 7.87K ohm	OTP modify
2010/01/05	53	Change PR196 to 2.55K ohm,PR204 to 8.66K ohm	circuit modify
2010/02/03	47	Change PC24,PC25,PC26 to 10U_1206,PR67 to 2.2 ohm PC153,PC154 to mount,	EMI request
		Add PC125,PC155	
2010/02/03	48	Change PR83,PR84 to 2.2 ohm,PQ27 to DTC115EUA_SC70-3 Add PC156	EMI request
		Change PL4,PL5 to SH16247AM10(4.7uH_H4.5)	circuit modify
2010/02/03	53	Add PC157,PC158	circuit modify
2010/02/26	46	Change PR31,PR33 to 23.7K ohm,PR34,PR40 to 11.3K ohm PD6,PD7 to mount	Thermal request EMI request
2010/02/26	47	Change PR45 to 20m ohm,PR68 to 24K ohm	cp point modify to 75W
2010/02/26	48	Change PL5 to SH000006380(4 mm high)	Thermal request
2010/02/26	53	Change PC111,PC114 to 100U	circuit modify for noise issue
2010/03/16	47	Change PC24,PC25,PC26 to 4.7U_0805, PC153,PC154 to unmount,	For PCB noise issue
2010/03/18	53	Change PC157,PC158 to mount,PC113,PC141 to unmount	circuit modify for camera noise issue
2010/04/02	49	Change PR98 to 10.5K ohm	circuit modify(cut in AON6718L)
2010/04/02	50	Change PR122 to 15K ohm,PC83 to 0.22uF	HW request
2010/04/02	51	Change PR132 to 12.1K ohm	circuit modify(cut in AON6718L)
2010/04/02	53	Change PC113,PC141 to mount	EMI request (for ISN)
2010/04/02	54	Change PR255 to 9.76K ohm	circuit modify(cut in AON6718L)

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PIR (Product Improve Record)

NALAA LA-6042P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	NO	DATE	PAGE	MODIFICATION LIST
1	2009/12/14	41	Delete R402, PCH_SUSPWRDN connect to EC directly	32	2009/12/22	43	Change H36, H37 footprint from H_3P8 to H_3P3
2	2009/12/14	43	Change JLEDB pin define as customer request	33	2009/12/22	25,41	Change Net name from PWRME_CTRL to PWRME_CTRL#
3	2009/12/14	30	Delete R222 and net PCH_GPIO45, PCH GPIO45 connector to GND for LVDS_SEL (Dual-Channel)	34	2009/12/23	16	Change CV114, CV116 from polymer cap to OSCON cap (SF000002000, H=5.9)
4	2009/12/14	34,35,39	Delete JODDB, JBT and JUSBB support pin	35	2009/12/23	36	Change control circuit of BT/WLAN combo Mini Card
5	2009/12/14	43	Change JPOWER Pin2 from GND to NC				a. Delete R22 and Net BT_PWR#_R at JWLAN pin5
6	2009/12/14	37	Add schematic for co-lay Giga LAN				a. Add Q25 and Net BT_CTRL at JWLAN pin5
			a. Add CL10 at +3VLAN	36	2009/12/23	38	Change RA26 from resistor 33_0603 to L58 bead 300 ohm FBMA-L10-160808-301LMT (SM010017710)
			b. Add CL23, CL24, CL25 at +LAN_VDD10	37	2009/12/24	24	Add R228 and HDMI_HPD_R at U9 pin1 to prevent ESD issue
			c. Add RL11 PD resistor at Pin15	38	2009/12/25	21	Add PJ6 between +3VS and +3VS_DELAY
			d. Add BOM structure 8105E@ at UL1	39	2009/12/25	45-55	Update PWR portion
			e. Change Transformer design for Giga LAN	40	2009/12/28	16	Change CV114, CV116 P/N from SF000002000 (330U,6.3V,15m ohm) to SF000002000 (390U,2.5V,10m ohm)
7	2009/12/14	22	Change U5 (CLK Gen) P/N from SA00003HQ00 to SA00003HQ10	41	2009/12/28	8,9,11,16,20	Change C159, C216, C217, CV78, CV290 footprint from C_PXC6P3VC220MF60 to C_MP2VU390MC5R7
8	2009/12/14	39	Change DA4, DA5 footprint from BJDLC05_SOT23-3 to PACDN042Y3R_SOT23-3	42	2009/12/28	35	Change R44 BOM structure from BT@ to @
9	2009/12/15	36	Add R22 and Net BT_PWR#_R at JWLAN Pin5 for BT/WLAN combo Mini Card	43	2009/12/28	30	Update Note for GPIO39,45,57 and project ID
10	2009/12/15	25	Change U13 (PCH ROM) footprint from WIESO_G6179-100000_8P to M25P80-VMW6TP-S0843, and delete BOM structure	44	2009/12/28	34	Change JODDB footprint from P-TWO_161021-12021_12P-T to ACES_88058-120N_12P-T
11	2009/12/15	34,39	Change U14, U15 P/N from SA00002XX00 to SA000033H00	45	2009/12/28	14	Add test pad T11 at UV1.AM14
12	2009/12/15	43	Change H36, H37 footprint from H_3P3 to H_3P8	46	2009/12/28	45-55	Update PWR portion
13	2009/12/15	35	Reverse JBT pin definition	47	2009/12/30	6	Change C4 from SE068102J80 to SE074102K80, keep @
14	2009/12/16	31	Add C473 (SF000002000) on +1.05VS plane for PWR request	48	2009/12/30	35	Delete R361 BOM structure for BT/WLAN combo card
15	2009/12/16	45-55	Update PWR portion	49	2009/12/30	37,43	Change LAN IC P/N
16	2009/12/16	5	Delete JXDP support pin				a. RTL8105E change from SA00003PO00 to SA00003PO10
17	2009/12/16	43	Add M92 XTX (SA00002YX00) for BOM control				b. RTL8111E change from SA00003PT00 to SA00003PT10
18	2009/12/16	13-18	Modify circuit for co-lay M9X	50	2009/12/31	43	Change M92 XTX P/N from SA00002YX00 to SA00002YX30
			a. Add BOM structure at RV133, RV33, LV33, CV308, CV309, CV310, LV34, CV311, CV312, CV313, LV35, CV314, CV315, CV316, LV36, CV317, CV318, CV319, LV30, CV302, CV303, CV304, LV31, CV305, CV306, CV307, LV28, RV41, RV42, RV45, RV46, RV56, RV54, RV132, CV206, RV59, CV320, CV321, RV57, RV58, RV48, RV49, RV50, RV53, RV55	51	2010/01/04	29	Change R281 from 22_0402 to 33_0402 per EMI request
			b. Add LV37 at +SPV10 and connect to +VGA_CORE	52	2010/01/04	41	Remove BOM structure from R377 and C443, Change C443 from 22P_0402 to 10P_0402 per EMI request
19	2009/12/16	14,18	Add BOM structure for GPU work around	53	2010/01/04	39	Change LA2, LA3, LA4, LA5 from 0_0603 to FBMA-L11-160808-800LMT_0603 (SM010015410) per EMI request
			a. Add BOM structure at RV19, RV16, RV39, XV1, LV32, CV117, UV20, RV56				
			b. Delete BOM structure from RV23				
20	2009/12/16	20	Change 2PCS@ to 4PCS@				
21	2009/12/16	40	Change CC2 from 0.1u to 100P (SE071101J80), and add BOM structure @				
22	2009/12/16	8	Change C144 from SF000002000 (390U, H5.9) to SF000002Z00 (330U, H4.5)				
23	2009/12/17	43	Change JPOWER footprint to ACES_85201-0405N_4P (ZIF_上接點)				
24	2009/12/17	35	Change JTPB footprint to P-TWO_161011-04021_4P-T (NO ZIF), and reverse pin definition				
25	2009/12/17	43	Change JLEDB footprint to ACES_85201-1605N_16P (ZIF_上接點)				
26	2009/12/17	39	Change JUSBB footprint to ACES_85201-20051_20P (ZIF_上接點)				
27	2009/12/17	13-22	Delete work around circuit of GPU				
			a. Delete RV40, CV117, UV20, RV39, XV1, LV32, RV16, RV19				
			b. Delete Net ROMSCK_GPIO10, GPIO24_TRST#, GPIO26_TCK, GPIO27_TMS				
			c. Change +3VS of VGA to +3VS_DELAY				
			d. Add +3VS_DELAY circuit				
28	2009/12/17	14	Change RV26 from 60.4ohm to 47.5ohm (SD00000G900)				
29	2009/12/17	43	Delete H15				
30	2009/12/21	45-55	Update PWR portion				
31	2009/12/22	22	Swap pin of JLVDS to prevent burn issue				
			a. +LCD_INV : Change pin from Pin35 to Pin40				
			b. BKOFF#_R : Change pin from Pin40 to Pin33				

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NALAA LA-6042P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST
1	2010/01/28	8	Remove BOM structure from C122 and delete C148
2	2010/01/28	37	Co-lay UL3 16-Pin Transformer for 10/100 (SP050005V00)
3	2010/01/28	38	Change UA1(CODEC) P/N from SA00003QR00 to SA00003QR10
4	2010/01/28	41	Add R37 10K pull-down resistor at VR_ON to avoid leakage for CPU_CORE
5	2010/01/28	27	Change U12 P/N from SA007080B90 to SA007080100
6	2010/01/28	21	Change PJ6 from Jump to R_0603 resistor R46 (SD013000080)
7	2010/01/28	18	Change RV57, RV58, CV320, CV321 BOM structure from MANHA@ to @
8	2010/01/28	34	Change D18 P/N from SCA00000A00 to SC600001600 per ESD request
9	2010/01/28	22,35,39,43	Change D19, D57, D58, DA4, DA5 P/N from SCA00000G00 to SCA00001A00 per ESD request
10	2010/01/28	39	Change LA2, LA3, LA4, LA5 footprint from R_0603 to KC_FBMA-L11-160808-800LMT12P
11	2010/01/28	32	Add BOM structure @ at C2, C7, U54
12	2010/01/28	41	Change U19(EC) from SA00001J80 to SA00001J5A0 and Change EC strap pin from R125 to R124
13	2010/02/01	39	Swap L and R pin definition
14	2010/02/01	25	Reserve D20 and R126 on RTC charge circuit
15	2010/02/02	43	Change M92-XTX P/N from SA00002YX30(R1) to SA00002YX50(R3)
16	2010/02/03	5	Add C414 at Peci for prevent noise issue
17	2010/02/03	34,39	Change U14, U15 from SA000033H00 to SA00002XX00
18	2010/02/03	8	Remove BOM structure from C117, C118, C119, C127, C128, C129, C150 and add C158
19	2010/02/03	45~55	Update Power portion
20	2010/02/04	34,39	Change U14, U15 footprint from RT9711CPB_SOT23-5 to RT9715BGS_S08
21	2010/02/08	37	Change LL1 from SHI00004T00 to SHI0000AA00 for common design
22	2010/02/08	37	Change CL13 from SE000000I10 to SE093475K80 for common design
23	2010/02/08	23	Change C238, C239, C240, C241, C242, C243 from SE07122AC80 to SE07147AC80 per EMI request

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NALAA LA-6042P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST
1	2010/02/09	25	Delete D20 and R126 on RTC charge circuit
2	2010/02/26	38,41	Add Net EC_MUTE# between U19.Pin83 and UA1.Pin4
3	2010/02/26	38,41	Add RA13 and RA29 at EC_MUTE#
4	2010/02/26	37	Change CL13 from SE093475K80 (0805) to SE107475K80 (0603)
5	2010/02/27	35,43	Change SW2, SW4 P/N from SN100000F00 to SN100002Y00 for cost down
6	2010/02/27	43	Add BOM structure @ at SW2 (Debug Button) due to PreMP
7	2010/03/01	38	Change EC_MUTE# pull-up from +5VALW to +5VS
8	2010/03/01	5	Add BOM structure @ at C414
9	2010/03/05	14	Add test point T12 at UV1.AK23, T13 at UV1.AL24 for AMD request
10	2010/03/09	38	Delete RA13 and un-mount CA16 for S3 resume and cold boot noise issue
11	2010/03/12	8	Change C144 PN from SF000002Z00 to SF000002M00 for 2nd source list common
12	2010/03/12	6	Change U1 PN from SA00002XA00 to SA000035G00 for 2nd source list common
13	2010/03/15	41,43	Add R103, C218 at LID_SW#_R for prevent ESD damage
14	2010/03/16	38	Change CA12,RA12,CA18 connect from GND to AGND
15	2010/03/17	40	Delete RC2,RC3,CC7,CC8 and add RC22,RC24,CC9,CC10 for EMI SD card issue
16	2010/03/22	22	Change C213 from SE070104Z80 to SE000000K80 for prevent noise coupling
17	2010/03/22	45~55	Update Power schematics
18	2010/03/30	34	Add BOM structure @ at D18 (EMI test PASS can remove it)

NO	DATE	PAGE	MODIFICATION LIST
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